Specialized Accelerators and Compiler Flows: Replacing Accelerator APIs with a Formal Software/Hardware Interface

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Abstract

Specialized accelerators are increasingly used to meet the power-performance goals of emerging applications such as machine learning, image processing, and graph analysis. Existing accelerator programming methodologies using APIs have several limitations: (1) The application code lacks portability to other platforms and compiler frameworks; (2) the lack of integration of accelerator code in the compiler limits useful optimizations such as instruction selection and operator fusion; and (3) the opacity of the accelerator function semantics limits the ability to check the final code for correctness. The root of these limitations is the lack of a formal software/hardware interface specification for accelerators.

In this paper we use the recently developed Instruction-Level Abstraction (ILA) for accelerators to serve this purpose, similar to how the Instruction Set Architecture (ISA) has been used as the software/hardware interface for processors. We propose a compiler flow termed D2A using the ILA and present a prototype that demonstrates this flow for deep learning (DL) applications. This prototype compiles programs from high-level domain-specific languages, e.g., PvTorch and MxNet, to multiple target accelerators with no target-specific extensions to the application or compiler thus demonstrating application portability. It includes compiler optimizations through instruction selection using equality saturation-based flexible matching. Finally, we demonstrate checking the correctness of the resulting code through both formal verification of individual matched operations, as well as fully automated simulation-based validation of complete applications. The evaluation of the prototype compiler is based on six different DL applications and three different accelerators. Overall, this methodology lays the foundation

Keywords: DSL, Compiler, Accelerator

1 Introduction

Hardware specialization is the main technique for improving power-performance efficiency in emerging compute platforms. By customizing compute engines, memory hierarchies, and data representations [12, 21, 43], hardware accelerators provide efficient computation in various application domains like artificial intelligence, image processing, and graph analysis [15, 28–30, 61, 87]. At the same time, there is a growing trend in using domain-specific languages (DSLs) for boosting development productivity, e.g., TensorFlow for deep learning [1], Halide for image processing [59], and GraphIt for graph applications [88]. However, there are critical gaps in bridging these two distinct system trends in the current compilation flows that start from high-level DSLs and target accelerator-rich platforms. ¹

Large industrial teams invest substantial resources to address DSL-to-accelerator mapping challenges via bespoke infrastructure [38, 39]. For smaller teams, like in the academic research community, these gaps make end-to-end evaluation of new accelerator designs prohibitively difficult; many recent papers on accelerator designs only evaluate on small application snippets, e.g., individual layers of deep neural networks [9, 23–25, 37, 56, 63, 64, 66, 71, 80, 81]. Unfortunately, an accelerator's results for application snippets are often *not* predictive of its influence on overall system behavior, e.g., due to cumulative effects of custom numerical representations — engineers need the ability to easily

for integrating accelerators in compiler flows using a formal software/hardware interface.

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¹Note that there are two different compilation problems that DSL compilers tackle: (1) adding compiler support for a given custom accelerator, and (2) generating the accelerator design to be implemented on an FPGA as part of the compilation [11, 32, 42, 55, 67, 79]. This paper deals with the former.

```
#define HWREG(addr) (*((volatile uint128_t*)(addr)))
2
    union buffer128 {
    uint128_t v128;
    int64x2 t v64:
4
5
    } buf;
6
7
    // FlexASR API: Layer Recude (max/min/mean pooling)
    bool FlexAsrLayerReduce(uint64_t* arg1, /* ... */) {
8
9
    // set up inputs and arguments
10
    buf.v64[0] = 0xC9A8070100CA8801;
11
    buf.v64[1] = 0x09D1008100810000;
    HWREG(0xA0500000) = buf.v128; // internal buffer[0]
12
13
14
    // configure and invoke operation
15
    buf.v64[0] = 0x0101000000010001;
    buf.v64[1] = 0x0000000200000001;
16
17
    HWREG(0xA0700010) = buf.v128; // global buffer control
    buf.v64[0] = 0 \times 00000000000000001;
    19
20
    HWREG(0xA0400010) = buf.v128; // memory manager config
    21
    22
    HWREG(0xA0000010) = buf.v128; // invoke operation
23
    // wait and retrieve results from the buffer
24
25
    sleep(5):
    buf.v128 = HWREG(0xA0500000);
27
    // ...
28
    }
```

Figure 1. Snippet of the FlexASR device driver [71]. Through MMIO commands, the driver first stores input arguments, e.g., weights, in the accelerator's internal buffer (lines 10 to 13). It then sets up the configuration such as tensor dimension and vector size (lines 15 to 20). Finally, it triggers the operation (line 23) and retrieves the result (starting line 26).

validate complete applications compiled onto accelerator platforms. This is lacking in current prevalent practice.

1.1 Prevalent Practice: Accelerator Drivers/APIs

Effective accelerator utilization requires offloading application computations to those supported by accelerators. In current practice, this is generally accomplished by manually crafting device drivers to provide "hardware function calls" for specific operations. This essentially provides an application programming interface (API) for accelerators, where each hardware function call consists of low-level accelerator invocation commands that configure, initiate, and check/return the results. Figure 1 shows an example hardware function call, in which a layer reduction operation is implemented by a sequence of memory-mapped input/out-put (MMIO) loads/stores from the host processor to invoke the FlexASR accelerator [71]. This MMIO-based API is the prevalent mechanism for accelerator invocation.

Generally, hardware function calls are manually added by application programmers, or they can be added by compilers via handcrafted accelerator-specific extensions. Such bespoke compiler extensions demand tedious effort and deep expertise in the hardware and the compilation stack. In practice, this limits end-to-end deployment of DSLs to accelerator-rich platforms within reach for only a few — large enterprises that can afford teams of hardware, software, and system experts for high-value applications [10, 22, 39]. Further, this API-based approach has three critical gaps in mapping applications from DSLs to accelerator-rich platforms:

- G1 Lack of portability. Hardware function calls implemented in device drivers contain MMIO loads/stores for accelerator invocation, but these low-level commands work only for a specific processing platform. When these calls are manually added by an application programmer, the application is not portable to new accelerator platforms. When these are added by a compiler through bespoke extensions, this task requires significant acceleratorspecific restructuring of the compiler. This is challenging due to: (1) the mismatch between fine-grained compiler intermediate representation (IR) intrinsics and coarsegrained accelerator operations (that are often used to deliver power-performance efficiency), and (2) the lack of a formal software/hardware interface specification for the accelerator that can be leveraged to automate this matching. This limits portability across both compiler frameworks and hardware platforms.
- G2 Lack of integration into standard compiler flows. Unlike general-purpose processors which have the ISA as the software/hardware interface, accelerators lack a formal software/hardware interface specification which makes the accelerator APIs opaque to the compiler stack. This makes it challenging to integrate them in standard compiler flows. For example, standard techniques for instruction selection [7] become challenging with a "blackbox" API, which provides little flexibility in selecting and reusing parts of these APIs. The fixed API also limits automation in exposing potential optimizations, e.g., operator fusion that may minimize data transfers.
- G3 Lack of ability to validate compilation results. Accelerators often incorporate novel techniques such as custom memory management schemes and numeric representations (referred to as numerics) to improve computational efficiency. However, existing compiler platforms do not readily support these unconventional features, which can lead to the generation of inefficient or even incorrect code. Unfortunately, the lack of a formal software/hardware interface specification of accelerator operations makes it very difficult to validate compilation results. In current practice, this is done using software/hardware co-simulation with an FPGA emulation of the accelerator or with a low-level register-transfer level (RTL) model for the accelerator. The former incurs significant engineering overhead, and the latter is very slow, making validation for full applications unrealistic.

In practice, validation using RTL co-simulation is performed only for individual accelerator-supported operations. This is insufficient to determine if small deviations at the operation level (e.g., due to different numerics) lead to acceptable results at the application level. Further, the need for a fully functional RTL model limits early stage software/hardware co-design, i.e., software development before the hardware is implemented.

The lack of a formal software/hardware interface specification that provides the semantics of individual accelerator operations is the root inadequacy across the three gaps. In this work, we propose the D2A (short for "DSLs to Accelerators") methodology which addresses these gaps via the use of an ISA-like formal model for accelerators, instead of using API-supported hardware function calls. The formal semantics of the accelerator operations are provided through an accelerator instruction set. This formal model and the finergrained, instruction-level control it provides (in contrast to API calls) facilitates standard compiling techniques (e.g., instruction selection and optimization), facilitates portability, and enables validation of compilation results.

1.2 D2A Methodology: Key Ideas

Identifying the computation in the application that can be offloaded to the accelerators is effectively seeking mappings between compiler IR intrinsics and the accelerator operations such that they are functionally equivalent and lead to performant code. (Note that in certain domains like machine learning, small numerical differences may not affect the application-level results, such as a classification category, so notions of "equivalence" should reflect this property.) While the semantics of the accelerator operations is available in the hardware RTL model, this is too low-level for the compiler to target directly and thus not an option. In the D2A methodology, we use the Instruction-Level Abstraction (ILA) [36], for this purpose. The ILA, like the ISA for processors, provides a software/hardware interface specification for accelerators. It bridges the gap between the compiler IR intrinsics on one hand and the accelerator operations on the other — providing the basis for specifying IR-accelerator mappings.

Compiler IR-Accelerator Mappings using ILAs. The ILA model of an accelerator provides formal semantics at its software/hardware interface through a *lifting* of the accelerator operations in the form of a set of instructions, each of which reads/updates the accelerator architectural state. Similarly, the IR intrinsics can be defined as instructions that update program state. This provides a uniform model on both sides — the IR side and the accelerator side — in the form of instructions. We specify the mappings as pairs of *program fragments*, where a program fragment comprises a sequence of instructions. Unlike API calls or RTL models, program fragments using accelerator ILA instructions capture the underlying accelerator operation semantics while

abstracting out low-level hardware implementation details. Further, these program fragments provide the flexibility to specify mappings at different levels of granularity — this helps bridge the granularity mismatch which may exist between IR intrinsics and coarse-grained accelerator operations.

Instruction Selection and Optimization. With the instruction semantics specified by an ILA, the D2A methodology facilitates standard instruction selection and optimization techniques in compilers. In this work, we use term rewriting for instruction selection, i.e., using compiler IR-accelerator rewrites to map IR intrinsics to accelerator instructions [3, 7, 20]. Specifically, we utilize equality saturation to optimally match equivalent rewrites of the program and therefore reduce the need for manual program restructuring (addressing gaps G1 and G2) [69, 74]. Further, the compiler IR-accelerator mappings have finer-grained knowledge and control of accelerator operations through the instruction-level interface provided by ILAs. This enables optimizations that require understanding of accelerator behavior, e.g., operator fusion for reducing data movement (addressing gap G2).

ILA-based Compilation-Results Validation. We use the term compilation-results validation for checking that the results of the compilation are correct, i.e., functionally equivalent or with acceptable deviation when there are differences in numerics. This may be done at the level of a single accelerator-supported operation, i.e., checking the correctness of compiler IR-accelerator mappings, or for the entire application. The formal semantics of the ILA instructions provides the foundation for proof-based formal verification or simulation-based validation. This enables systematic endto-end compilation-results validation as well as early-stage software/hardware co-design (addressing gap G3).

D2A Compilation Flow. The overall compilation flow using the D2A methodology is shown in Figure 2. We first translate the application program, provided in a high-level DSL, into the compiler IR. Next, we perform equality saturation to search a large space of equivalent programs given the compiler IR-accelerator mappings (along with general-purpose rewrite rules). Based on a given cost function, we then extract the lowest-cost program and pass it on for code generation, where each accelerator instruction is subsequently lowered to the corresponding MMIO load/store command. This generated program executes on the host processor and invokes accelerator operations through MMIO commands. (Note that the ILA modeling and the validation of the IR-accelerator mappings are omitted from this figure.)

1.3 Prototype Implementation and Case Studies

As a demonstration of the D2A methodology, we have implemented an end-to-end compilation flow for deep learning (DL) applications by integrating it with an existing compiler flow. Specifically, our prototype compiler utilizes the DSL

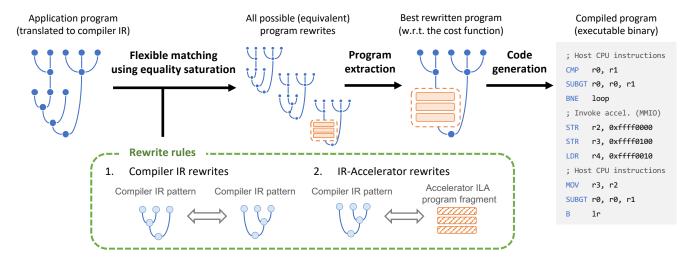


Figure 2. D2A compilation flow overview.

front-end and the code-generation capability provided by the TVM framework [14]. For instruction selection, it leverages the rewrite rules and the equality saturation engine provided by Glenside and egg [68, 83]. The ILA-models of accelerators, the validation of IR-accelerator mappings, and compilation-results validation at the application level are powered by ILA-based methods in ILAng [35].

We show the generality of the D2A methodology through multiple case studies. At the front-end, we consider six DL applications for language processing and image recognition, e.g., Transformer [77] and ResNet [31]. For the target accelerators, we add support for three custom accelerators that provide hardware operations at different levels of granularity: VTA [50] is a fine-grained accelerator for general tensor operations; HLSCNN [81] is a coarse-grained accelerator providing 2D convolutions; FlexASR [71] is an accelerator for speech recognition, specializing in coarse-grained operations such as a long short-term memory (LSTM) layer.

We added support for the three accelerators — developed their ILA models, provided compiler IR-accelerator mappings for operations supported by them, and validated all the mappings. Note that this work for supporting a new accelerator is a one-time effort that can be reused across different applications. Our prototype compiler successfully compiled all six DL applications (developed by different teams and programmed in different DSLs) for exploiting the three custom accelerators. Our prototype and case studies demonstrate the key ideas in the D2A methodology for end-to-end compilation with validated results. We do not claim this work provides a complete, fully optimized compiler for custom accelerators; rather, it establishes the foundations for validated compilation for such targets through the use of a formal instruction-level software/hardware interface for accelerators.

1.4 Contributions

Overall this paper makes the following contributions:

- We present the D2A methodology that uses an instructionlevel formal software/hardware interface specification for an accelerator, which abstracts away low-level implementation details while providing a formal hardware semantics with the following capabilities:
 - It bridges the granularity gap between compiler IR intrinsics and accelerator operations with flexible mappings between instruction-level program fragments.
 - It enables integration into standard compiler flows and the application of standard techniques like instruction selection and optimization.
 - It provides for end-to-end validation of compilationresults for accelerator-extensible compilers.
- We describe a prototype² that implements the D2A compilation flow on top of open-source frameworks TVM, Glenside, egg, and ILAng.
- We provide a set of case studies that demonstrate:
 - portability: through compiling six DL applications (programmed by different teams in different DSLs)
 - extensibility: through adding support for three custom accelerators which provide operations at different levels of granularity.
 - compilation-results validation: for both IR-accelerator mappings, and at the application-level. The latter demonstrates how this methodology exposed several accuracy issues due to custom numerics.

This article is organized as follows. In Sections 2 and 3, we explain the D2A methodology and our compiler prototype, respectively. We then describe the case studies and evaluation results in Section 4. Future work, related work, and conclusions are discussed in Sections 5, 6, and 7, respectively.

²Our prototype will be released under a permissive open-source license.

2 D2A Methodology

In this section, we explain three key aspects of the D2A methodology: (1) adding accelerator support by specifying mappings between compiler IR intrinsics and accelerator operations, (2) compiling applications by searching within input programs for computations supported by accelerators, and (3) ensuring compilation-result validation and supporting early-stage software/hardware co-design.

2.1 Specifying IR-Accelerator Mappings using ILAs

The ILA is an ISA-like formal model for specifying the functional behavior of accelerators. It generalizes the notion of instructions to accelerators and provides a modular functional specification as a set of instructions. Like processor ISAs, it does so by specifying how each instruction updates software-visible (viz., architectural) state while abstracting out implementation details.

- **2.1.1** Accelerator ILA. We develop the ILA formal model for an accelerator by following the methodology proposed in prior work [36]. Each instruction of an accelerator ILA corresponds to a command at the accelerator interface, i.e., an MMIO load or store command. The ILA captures formal semantics of accelerator behavior by specifying how each instruction reads/updates the architectural state variables. Essentially, the ILA is a modular (per-instruction) operational specification of an accelerator. Figure 6 in Appendix C provides an accelerator ILA example.
- **2.1.2 Compiler IR ILA.** While the ILA is primarily intended to serve as the formal model for accelerators, it is convenient to also use it to formally model compiler IR intrinsics. We develop the compiler IR ILA by following the approach used in prior work for the NVidia parallel execution thread (PTX) programming model [86]. Each instruction of a compiler IR ILA corresponds to an IR intrinsic and specifies its operational behavior in terms of how it updates program state. Modeling both the compiler IR and accelerators using ILAs provides a uniform model on both sides, and enables the use of the ILAng toolkit for their verification/validation.
- **2.1.3 IR-Accelerator Mappings.** Due to the granularity gap between the IR instrinsics and the accelerator operations, it is often not possible to construct a one-to-one mapping between the compiler IR and the accelerator operations. Instead, on each side (the compiler IR and the accelerator), we consider a program fragment that comprises a sequence of instructions defined by the associated ILA model. The program fragments provide a basis for *many-to-many instruction mappings between the two sides*, providing flexibility that is key to addressing the granularity mismatch challenge.

The specification of the mappings starts from the accelerators — based on the given accelerator, we provide an IR-accelerator mapping for each accelerator operation. This bottom-up approach is a one-time effort for each accelerator,

```
// (a) Compiler IR pattern
%1 = nn_dense(%2, %3)
%4 = bias_add(%1, %5)
        Verification task 1 (VT1)
         • Compiler IR ILA vs. compiler implementation
            Modular, per-instruction check
// (b) Compiler IR ILA program fragment
comILA.nn dense %arg1 %arg2 %arg3
comILA.bias_add %arg4 %arg1 %arg5
        Verification task 2 (VT2)
          Program fragments equivalence checking
           Sequence to sequence checking
// (c) Accelerator ILA program fragment
accILA.cfgPELayDims %dim1 %dim2
accILA.cfgPEManager %addr1 %addr2
accILA.cfgPEActions %addr3 %addr4
accILA.cfgGBMemIdxs %midx1 %midx2
accILA.cfgGBControl %opcode
accILA.triggerStart
        Verification task 3 (VT3)
           Accelerator ILA vs. RTL implementation
           Modular, per-instruction check
// (d) Accelerator invocations (MMIOs)
WR 0xA1040010, 0x0100102040001001
WR 0xA1040020, 0xFFFF49DE5F5C0010
WR 0xA1080010, 0x010210403301FFFF
WR 0xA0040010, 0x0000000102040001
WR 0xA0070010, 0x004008101000000A
WR 0xA0000010, 0x00000000000000001
```

Figure 3. Verification tasks and the IR-accelerator mapping for a linear-layer operation supported by FlexASR [71]. (The mapping is simplified for a clearer presentation. See Figure 5 in the Appendix for the complete mapping.)

requires no knowledge of the input program, and is the key for modular and extensible compilation.

Figure 3 shows an example of an IR-accelerator mapping for a linear layer operation for the FlexASR accelerator [71]. The program fragments of the compiler IR and the accelerator are shown in parts (b) and (c), respectively. As discussed, each instruction of the compiler IR ILA corresponds to one IR intrinsic, which is reflected in parts (a) and (b). Similarly, each instruction of the accelerator ILA corresponds to one command at its MMIO interface, as shown in parts (c) and (d).

2.2 Flexible Matching using Equality Saturation

Given the IR-accelerator mappings and an input program, the next step in the D2A methodology is to identify computations in the input program that can be offloaded to equivalent accelerator operations. We approach this task by utilizing term rewriting techniques — given a set of syntactic rewrite rules $(\ell \to r)$, rewrite instances of pattern ℓ in the input program with pattern r where applicable [3, 7, 20, 69, 74]. In term rewriting systems, the application of rewrite rules is

correct by construction as long as the rules preserve semantic equality. This provides for modular correctness checking through checking the individual rewrite rules.

Classic term rewriting systems often suffer from the phase ordering problem (i.e., the order in which rewrites are applied affects final performance) and thus require careful ordering [82]. In D2A, we utilize the equality saturation technique to mitigate phase ordering problems [69, 74].

Equality Saturation. Given an input program *p*, equality saturation repeatedly applies the given rewrite rules to explore all equivalent ways to express *p* (with respect to the rules). It utilizes the *e-graph* data structure to efficiently represent an exponentially large set of equivalent program expressions [52, 53]. Upon reaching a fixed point, i.e., when no application of any rewrite rule can introduce a new program expression, it extracts the optimal rewritten program according to a given cost function. This provides for searching over the space of all possible rewrites and finding the representative most suitable for the given purpose without sophisticated ordering considerations.

2.2.1 IR-Accelerator Rewrites. Based on the provided IR-accelerator mappings, we derive a set of rewrite rules where the left-hand side of the rule is the compiler IR pattern and the right-hand side is the corresponding accelerator instructions. Applying these rules, which we call the *IR-accelerator rewrites*, allows replacing the computations that are exact syntactic matches to the compiler IR pattern specified in the mappings by the corresponding accelerator operations. We call this *exact matching*.

2.2.2 Flexible Matching and Compiler IR Rewrites.

Exact matching provides a baseline matching capability but may be limited in practice because there is often no canonical IR expression to represent a program. Therefore, the input program can have constructs that are syntactically different from the left-hand side of the IR-accelerator rewrites but are semantically equivalent to the pattern. For example, in the IR-accelerator mapping shown in Figure 3, we specify the compiler IR pattern for a linear layer (as an S-expression):

(bias_add (nn_dense %a %b) %c).

However, a linear layer can be equivalently expressed as

(add (reshape (nn_dense %a %b) %s) %c)

when %c is a vector, for certain shapes %s. This prevents exact matching from identifying potential accelerator calls.

Rather than enumerating various semantically equivalent IR-accelerator mappings, we include another set of rewrite rules that we call *compiler IR rewrites*. Each compiler IR rewrite transforms an IR pattern into another IR pattern, e.g., from the second to the first linear-layer IR pattern above, without replacement by accelerator instructions. These general-purpose rewrite rules do not depend on the input program nor on the accelerator, but help expose more potential matches.

We refer to this as *flexible matching*, as it enables finding matches that may be missed by exact matching.

2.3 ILA-Based Compilation-Results Validation

The formal semantics of ILA instructions provides the foundation for validating compilation results. The D2A methodology does compilation results validation at two levels.

2.3.1 Checking IR-Accelerator Mappings. The use of term rewriting provides for modular validation — checking end-to-end compilation correctness by verifying individual rewrite rules. In D2A, we focus on the verification of IR-accelerator mappings from which IR-accelerator rewrites are derived. Checking and inferring rules between compiler IR patterns is not the focus of this paper [5, 48, 51].

Verifying an IR-accelerator mapping consists of three verification tasks, as illustrated in Figure 3, At the two ends, i.e., the compiler IR and the accelerator end, we check the equivalence through VT1 and VT3, respectively. In the middle, VT2 checks the equivalence between a compiler IR ILA program fragment and an accelerator ILA program fragment. This is an instruction-sequence-to-instruction-sequence verification, typically over short program fragments that correspond to operations instead of a whole application.

Proof-Based Formal Verification. The formal semantics of ILA instructions allows for formally verifying the IRaccelerator mappings. For VT1, the equivalence between compiler IR intrinsics and compiler IR ILA instructions can be checked using software model checking tools (e.g., CBMC and SeaHorn [18, 27]) by translating ILA models into software models, as has been done in prior work [34]. For VT2, the two program fragments can be encoded into Satisfiability Modulo Theories (SMT) formulas (e.g., via unrolling the instructions) and their equivalence checked using an SMT solver such as Z3 [19]. For VT3, the refinement checking between the accelerator ILA (specification) and the accelerator RTL (implementation) has been shown successfully in prior work [36] that leverages processor verification techniques [8, 47]. We provide a case study for VT2 in Section 4 that focuses on verifying equivalence of the operator definitions in the two program fragments over abstract data types, thus avoiding dealing with differences in numerics which are the focus of the simulation-based validation.

Simulation-Based Validation. The D2A methodology also supports checking VT1-3 through simulation-based validation. This is highly automated as the ILAng platform [35] can automatically generate an executable software model (in C++/SystemC) of a program of ILA instructions. These executable models capture the precise definitions of the numerics used by the accelerator. For VT1, the simulation of ILA instructions is checked against the execution of the corresponding IR intrinsics (i.e., the original compiler generated

code). For VT2, we compare the simulation of two ILA program fragments. For VT3, the ILA simulation can be checked against RTL simulation of the accelerator implementation.

2.3.2 Application-Level Co-Simulation. Verification at the application-level, e.g., examining the final accuracy of an inference model instead of its individual layers, is especially critical for exploiting accelerators that utilize custom data representations. While such accelerators gain power-performance efficiency by leveraging custom data types, they may introduce modest numerical mismatches at every operation. Thus, the IR-accelerator mapping validation for a pair of program fragments (§ 2.3.1) can at best check that the numerical differences for the computation in these fragments is within a certain range. Unfortunately, this provides no guarantee of the correctness at the application level and, therefore, requires the application-level co-simulation capability enabled by the use of the ILA models.

3 Prototype Implementation

As a demonstration of the D2A methodology, we have implemented an end-to-end compilation flow for Deep Learning (DL) applications by integrating with existing compiler frameworks. Figure 4 shows the workflow of our prototype.

DSL Front-End. TVM is a compiler framework for DL applications that provides various capabilities for expressing and optimizing DL applications [14]. Here, we make use of TVM's model importer as the front-end for DSL programs. The importer supports taking programs written in mainstream DL frameworks and interchange formats (e.g., ONNX [46], Py-Torch [57], and TensorFlow [1]) and translating them into Relay, the top-level IR used in TVM [62].

Flexible Matching. We leverage the egg library for equality saturation in our prototype [83]. First, the input program is translated from Relay to Glenside, a pure (side effect-free) tensor program representation that supports specifying rewrite rules for tensor programs [68]. Next, with both the compiler IR rewrites and IR-accelerator rewrites provided in Glenside, the equality saturation engine explores the space of possible rewrites as discussed in § 2.2. Upon reaching a fixed point, an optimal rewritten program is extracted based on a given cost function. Here, as a proof of concept, we implemented a cost function that maximizes the number of accelerator operations; we leave cost functions that best correspond to measures of performance for future work.

Code Generation. Once flexible matching completes, the extracted rewritten program is translated back to Relay where accelerator instructions are specially annotated. In our prototype, we use TVM's Bring Your Own Codegen (BYOC) interface to implement the generation of those accelerator instructions [16]. BYOC allows for invoking the target interface of a custom execution mechanism (e.g., an accelerator's

MMIO loads/stores) by having TVM's runtime defer execution to a user-specified runtime when it reaches an annotated portion of the program. Here, we implemented a custom runtime that invokes the accelerator implemented on an FPGA (§ 4.3.2) as well as the ILAng-generated simulators (see below), producing the necessary ILA instructions at run time. Such a just-in-time approach helps prototyping as it allows for easily inspecting intermediate values in the program and simplifies the implementation, but introduces overhead from communication between the TVM runtime and our custom D2A runtime. In principle, this overhead can be eliminated by using BYOC's ahead-of-time compilation mode.

ILA Modeling and Correctness Verification. We utilize ILAng, an open-source platform for ILA-based modeling and verification, for developing the ILA models and performing ILA-based verification/validation [35]. ILAng provides support for the following capabilities:

- 1. (a) manually specifying and (b) semi-automatically synthesizing an ILA model [70].
- 2. refinement checking between an ILA specification and an RTL implementation.
- automatic translation from semantics of ILA instructions to SMT formulas.
- 4. generating a sound executable simulator based on the operational semantics defined by the ILA model.

We use 1(a), 3, and 4 in this work.

4 Case Studies and Evaluation

We show the generality of the D2A methodology through multiple case studies.

4.1 Target Accelerators

We added support for three accelerators specialized for DL applications that provide hardware operations at different levels of granularity:

- FlexASR is an accelerator optimized for speech and natural language processing (NLP) tasks that supports various recurrent neural networks [71]. It uses a custom numeric datatype *AdaptivFloat* for boosting the accuracy of quantized computations [72].
- 2. **HLSCNN** is an accelerator optimized for 2D convolutions [81]. HLSCNN is designed to operate on 8/16-bit fixed point data, and the feature map tensors are expressed in the NHWC layout format for providing better performance through parallelization.
- 3. VTA is a parameterizable accelerator for tensor operations featuring a processor-like design with an ISA and configurable parameters [50]. It provides efficient hardware implementations of element-wise arithmetic operations as well as generalized matrix multiplication (GEMM).

The ILAs for FlexASR, HLSCNN, and VTA are approximately 5600, 1600, and 2100 lines of code, respectively — note that

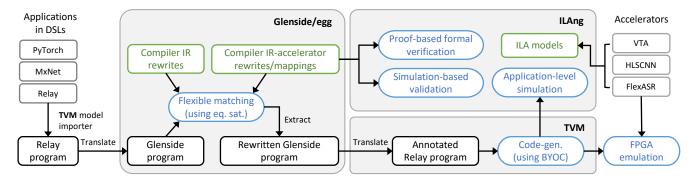


Figure 4. Prototype implementation of the D2A compilation flow.

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	Application Statistics						
1	Application	EfficientNet	LSTM-WLM	MobileNet-V2	ResMLP	ResNet-20	Transformer
2	Source DSL	MxNet	PyTorch	PyTorch	PyTorch	MxNet	PyTorch
3	#Relay Ops	232	578	757	343	494	872
Number of Static Accelerator Invocations using Exact Matching/Flexible Matching							
4	FlexASR	0/35	1/1	0/41	0/38	2/22	0/66
5	HLSCNN	35/35	0/0	40/40	0/0	21/21	0/0
6	VTA	0/35	36/36	1/41	38/38	2/22	66/66

Table 1. End-to-end compilation statistics.

these ILAs serve the dual purposes of enabling compilation via the D2A methodology as well as validating the RTL design. Additionally, the BYOC-based code generators and runtimes for these devices are approximately 450, 300, and 900 lines of code, respectively. Please see Appendix A for a complete list of supported operations for the three accelerators.

4.2 Target Applications

For our experiments, we considered six DL applications corresponding to common neural network models for language and vision tasks that contain operators supported by the three target accelerators. We selected applications with reasonable size for human inspection and in-depth analysis.

- EfficientNet is a recent convolutional neural network (CNN) designed for image classification that uniformly scales network width, depth, and resolution [73]. We chose it because it contains convolutions that could be accelerated by VTA and HLSCNN.
- 2. **LSTM-WLM** is a simple text generation application [84] implemented using an LSTM recurrent neural network architecture [26]. We chose this model because it contains an LSTM layer that could be accelerated by FlexASR. As detailed in Appendix B, we made a small modification to the model after importing into Relay to match the semantics of our FlexASR LSTM code generator, namely by not returning the final hidden and cell states (unused in this application).

- 3. **MobileNet-V2** is a commonly used CNN, designed for mobile and embedded vision applications, that uses depthwise separable convolutions [33, 65]. We chose MobileNet due to its wide use, especially on embedded devices.
- 4. ResMLP is a recent residual network, designed for image classification, comprised only of multi-layer perceptrons and no convolutional layers [75]. We chose this model because its preponderance of linear layers means it could be accelerated by VTA as well as by FlexASR (despite not being a language model).
- ResNet-20 is a CNN designed for image classification that applies identity mapping [31]. As with MobileNet, we chose ResNet for its common use in practice.
- Transformer is a language representation model comprised primarily of attention mechanisms [77]. We chose Transformer as a representative of recent NLP models in common use.

With the exception of the minor change for LSTM-WLM, all applications were mapped to accelerators *without any manual modifications*. Detailed parameters for these applications are given in Appendix B.

4.3 Evaluation: Compilation

We examined the portability provided by D2A through endto-end compilation using our compiler prototype. We took six DL applications, developed by different teams in different DSLs, and compiled them for the three target accelerators. Our compiler prototype successfully generated code that exploits the accelerators for supported computations. Furthermore, we demonstrate full-system deployment, running D2A-generated code on physical hardware through FPGA emulation.

4.3.1 Portability and Flexible Matching. Table 1 shows the compilation statistics of using exact matching and flexible matching. It describes the source language in which the application is programmed (Row 2) and the program complexity using the number of Relay operators as a proxy (Row 3). It reports the number of invocations to FlexASR, HLSCNN, and VTA when using exact/flexible matching in Rows 4-6. Note that some invocations (IR-acclerator mappings) correspond to multiple Relay operators; in particular, the 35-step FlexASR LSTM in LSTM-WLM is 566 operators and maps to *one* FlexASR LSTM instruction (a dramatic granularity mismatch between DSL and accelerator operations).

Our results demonstrate portability with the successful exploitation of accelerators for supported operations and provide evidence for the utility of flexible matching. For example, flexible matching revealed several offloads to Flex-ASR's linear layer in MobileNet-V2 by rewriting nn. dense to nn. dense followed by an add of a zero tensor. Also note that certain Glenside rewrites [68] that implement the im2col optimization [13] result in many more offloads to VTA in that table; this is due to 2D convolutions being rewritten into matrix multiplications. Hence, flexible matching allowed us to support 2D convolutions on VTA even though our prototype code generator did not explicitly implement 2D convolutions via VTA instructions. This is an example of *emergent effects* resulting from simple, reusable rewrite rules.

4.3.2 System Deployment and FPGA Emulation. To demonstrate the D2A flow on a real hardware platform, we synthesized, placed-and-routed the FlexASR accelerator on a Xilinx Zynq ZCU102 FPGA, which consumed 86% of the available LUT resources.3 We utilized the Xilinx SDK [85] to pass the accelerator instructions (MMIO commands) to the accelerator interface for invoking the supported operations. Specifically, we compiled and executed synthetic application programs in which LSTM layers and linear layers are offloaded to the FlexASR accelerator. This case study demonstrates the applicability of D2A in actual system deployment on a commodity hardware platform. Further, it shows that in the absence of compilation-results validation enabled by the D2A methodology, the need for a fully functional RTL model and the significant engineering overhead indeed limit early-stage software/hardware co-design.

4.4 Evaluation: Compilation-Results Validation

We want to check that the compiled program, in which parts of the computation are offloaded to accelerators, retains the

Table 2. Simulation-based validation results of checking IR-accelerator mappings (partial). The average relative error (Avg. Err.) and the standard deviation (Std. Dev.) of the errors are measured for simulation over 100 test inputs.

	Accelerator	Operation	Avg. Err.	Std. Dev.
1	VTA	GEMM	0.00%	0.00%
2	HLSCNN	Conv2D	1.78%	0.16%
3	FlexASR	LinearLayer	0.84%	0.29%
4	FlexASR	LSTM	1.21%	0.19%
5	FlexASR	LayerNorm	0.27%	0.20%
6	FlexASR	MaxPool	0.00%	0.0%
7	FlexASR	MeanPool	1.79%	0.28%
8	FlexASR	Attention	4.22%	0.09%

same functionality as intended with the IR semantics. Thus, we use the IR ILA specification as the reference for formal verification of the IR-accelerator mappings, and use an IR interpreter as the reference when running simulation at two levels: the operation level (for checking the IR-accelerator mappings) and the application level.

4.4.1 Checking IR-Accelerator Mappings. Modern accelerators often adopt custom numerics for achieving better power-performance efficiency. For example, in our cases, FlexASR and HLSCNN use the AdaptivFloat and 8/16-bit fixed point data types, respectively. This means checking the IR-accelerator mappings must account for the numerical differences. To separate the effect of numerics and focus on the definition of operations, we use abstract data types to formally verify the equivalence (demonstrated through a proof-of-concept case study). In addition, to precisely capture the numerical differences, we use simulation to compare accelerator executions (using an ILA simulator) against the IR semantics (using an IR interpreter).

Simulation-Based Validation. For checking the mappings through simulation, we generated 100 random test inputs and compared the outputs of the accelerator ILA simulator and that of an IR interpreter. The accelerator ILA simulators precisely model the data types used by the accelerators. Specifically, VTA, HLSCNN, and FlexASR use 8-bit integer, 8/16-bit fixed point, and AdaptiveFloat, respectively. For the IR interpreter, as a reference, we use 8-bit integer, 32-bit floating point, and 32-bit floating point when checking operations of VTA, HLSCNN, and FlexASR, respectively. These are respectively the closest standard datatypes to those used by these accelerators. The relative errors are measured using the standard Frobenius Norm [2] for the tensors as follows: $Error = \|Out_{ref} - Out_{acc}\|_F / \|Out_{ref}\|_F.$ Table 2 shows a selected subset of the validation results:

Table 2 shows a selected subset of the validation results: four IR-accelerator mappings (Rows 1-4) that are used in the end-to-end compilation (Table 1) and four additional

³Due to the significant engineering overhead of FPGA emulation, FlexASR is the only accelerator we deployed on an FPGA.

mappings for non-trivial operations (Rows 5-8). We omit validation results of other mappings, e.g., for trivial operations *add* and *max*. Columns 1 and 2 indicate the accelerator and the supported operation for each IR-accelerator mapping, respectively. Columns 3 and 4 provide the average relative error and the standard deviation, respectively, over the 100 test inputs. For mappings that are not affected by numerical differences, e.g., the VTA-supported GEMM, we see exact matches in the results. For other mappings, we see deviations caused by the custom numerics, especially for complex operations such as the attention operation for FlexASR.

Proof-Based Formal Verification. The key challenges in formally verifying mappings between fragments that represent DL computations include: (1) handling nested loops, for both compiler side and accelerator side, that iterate through tensor elements, and (2) relating tensor variables between the two sides which may employ various tiling mechanisms. As a proof-of-concept study, we considered the Relay and FlexASR fragments for the FlexASR MaxPool IR-accelerator mapping. These fragments both have 3+ nested loops, and the relation between the two fragments must account for a special customized tiling provided by FlexASR [71]. For this study, we considered equivalence of the fragments over fixed-sized tensors with symbolic data,4 and implemented verification using two methods: (1) bounded model checking (BMC) [6], and (2) program verification using constrained Horn clauses (CHCs) [40]. The BMC-based method unrolls all the loops in both fragments, which is straightforward but may fail to scale for large-sized tensors. The CHC-based method is given a product program of the two fragments and uses relational loop invariants, i.e., formulas that relate the two fragments at intermediate loop boundaries (details are beyond the scope of this paper). This avoids loop unrolling and can handle large tensors. Both methods use Z3 [19] as the underlying SMT solver.

While ILAng directly supports BMC, we manually created CHCs for the CHC-based method. We also supplied the relational invariants that capture the customized tiling of Flex-ASR. In future work, we plan to automate CHC generation, which will allow formal verification of other IR-accelerator mappings used in this paper. Table 3 shows the results for this case study for various dimensions of the 2D input matrix (Column 1), with runtimes of the BMC-based and CHC-based verification methods in Columns 2 and 3, respectively. The BMC-based method was able to verify equivalence of mappings with small-sized matrices, but timed out (with a 3-hour time limit) on the 16×64 matrix that was used for simulationbased validation. In contrast, the CHC-based method was faster than BMC and successfully verified mappings with larger matrices. These results are encouraging and demonstrate how the D2A methodology enables formal verification of key steps in the compilation flow.

Table 3. Formal verification case study: results for verifying the IR-accelerator mapping for FlexASR Max-Pool. Experiments were run on an Intel Core i7-5500U CPU (two 2.40GHz cores) with 8 GB RAM.

Matrix dim.	BMC verif. time (s)	CHC verif. time (s)	
2 × 16	443	38	
4×16	1976	37	
4×32	7954	146	
8×64	Timeout (>3 hrs)	1831	
16×64	Timeout (>3 hrs)	5177	

4.4.2 Application-Level Co-Simulation. With the validated IR-accelerator mappings, we want to check if minor deviations at the operation level will influence application-level behavior. Therefore, we performed application-level co-simulation on several applications which offload various computations to FlexASR and HLSCNN, the two accelerators that utilize custom numerics. Specifically, we examined LSTM-WLM and ResMLP, which offload to FlexASR the LSTM layer and linear layer operations, respectively. We also considered MobileNet and ResNet, which both offload 2D convolution and linear layer operations to HLSCNN and FlexASR, respectively. (We compiled to two target accelerators by including the IR-accelerator rewrite rules for both accelerators.)

We trained and validated the LSTM-WLM model using the WikiText-2 dataset [49]. The image classification models (MobileNet-V2, ResMLP, and ResNet-20) were trained and validated using the CIFAR-10 dataset [17]. Table 4 shows the application-level co-simulation results. Columns 1 and 2 describe the application and the target processing platform under evaluation, respectively. We provide a reference result (perplexity for the text-generation task and inference accuracy for vision tasks) in Column 3 by running the application on the host processor, i.e., not offloading to accelerators. The validation result using original accelerator designs, labeled "Original Result," is provided in Column 4. For cases where the "Original Result" was significantly poorer than the reference result, we reported it to the accelerator developers for their further investigation. When they provided an accelerator design modification to address this, we provide an updated result, using this modified accelerator, in Column 5. The average simulation time is reported in Column 6.

Case Study: ResNet-20 and MobileNet-V2. We reported the original validation results of ResNet-20, which were far from the 91.55% reference result, to the accelerator developers. We also provided statistics for each accelerator invocation (e.g., error accumulation, input and output ranges, etc.), gathered by our compiler prototype and ILA simulators. With the information, the accelerator developers were able to identify the root cause: weight data values in HLSCNN's 2D convolutional layers were heavily quantized by its 8-bit

⁴Formally modeling custom numerics is left to future work.

Table 4. Application-Level Co-Simulation Results. In each validation, we evaluated 2000 images (for vision tasks) or 100 sentences (for text generation) that were evenly sampled from the corresponding dataset. The original result is measured using original accelerator designs. The updated result is measured using modified designs provided by the accelerator developers.

Application	Processing Platform	Reference Result*	Original Result	Updated Result	Avg. Sim. Time [†]
LSTM-WLM	FlexASR	122.15 (perplexity)	257.39 (perplexity)	Reported	1min 10s
ResMLP	FlexASR	69.65% (accuracy)	10.65% (accuracy)	Reported	19min 15s
ResNet-20	FlexASR & HLSCNN	91.55% (accuracy)	29.15% (accuracy)	91.85% (accuracy)	14min 23s
MobileNet-V2	FlexASR & HLSCNN	92.40% (accuracy)	10.35% (accuracy)	91.20% (accuracy)	42min 26s

^{*} The reference result does not represent the best achievable accuracy/perplexity of the model on the given dataset. This table is intended for comparing the application-level results on different processing platforms.

fixed point data type due to a narrower value range. After updating the design by expanding the original 8-bit representation to 16 bits, the application-level result matched up to the reference result. The same tuning approach also resulted in improved accuracy for MobileNet-V2.

The results in Table 4 reaffirm the need for application-level validation, especially for accelerators utilizing custom numerics. However, without a portable end-to-end compilation flow, such application-level validation is prohibitively difficult for new accelerators. Through our case studies, we demonstrate how D2A provides systematic and automatic compilation-results validation at the application level and also show its usefulness in software/hardware co-design. Specifically, with the ILA, D2A provides quick design space exploration and numerics tuning without hardware engineering overhead (e.g., deploying to FPGA) in each hardware design iteration. Further, it provides handy debugging information and efficient simulation. (For FlexASR, we see a 30× speedup on average with the ILA simulator compared to RTL simulation using a commercial Verilog simulator.)

5 Discussion and Future Work

The D2A methodology establishes a foundation for an endto-end, validatable compilation flow for accelerator-rich platforms. Our prototype not only provides a working implementation, but also an experimental framework for future research in this area. Thus far, we have demonstrated how flexible matching, mapping validation, and application-level co-simulation are enabled by D2A. Below we discuss two example near-term extensions ripe for further exploration and inclusion in D2A-based frameworks.

5.1 Optimizing Data Transfers

As a motivating example, we consider an image processing application with a 2D max-pooling layer that we would like to offload to FlexASR. Suppose that the max-pooling layer uses a window with shape (4,4) and stride (2,2) and is used to downsample a 128×128 matrix into a 64×64 matrix. However, FlexASR does not directly support this window or stride size. Instead, it supports a related operation called

temporal max-pooling, which corresponds to 2D max-pool with a fixed window of shape (2, 1) and stride (2, 1). The following IR-accelerator rewrite rule represents an offloading of the temporal max-pooling operation, where the IR fragment is shown on the left of the arrow, and the FlexASR fragment on the right (?T in the pattern denotes the input matrix; fragments are shown as S-expressions).

```
1 | ; Rewrite rule for IR-accelerator mapping
2 | (map reduceMax (windows (2, 1) (2, 1) ?T)) ->
3 | (fasrMaxpLoad (fasrMaxpool (fasrMaxpStore ?T)))
```

By using flexible matching, our prototype found the following rewritten IR program for the 2D max-pooling layer:

```
1 | ; Rewritten IR program for window (4, 4), stride (2, 2)
2 | ; T denotes the input to the 2D max-pooling layer
3 | ; S is the shape of the output of the 2D max-pooling layer
4 | (reshape (map reduceMax (windows (2, 1) (2, 1))
5 | (map reduceMax (windows (2, 1) (2, 1))
6 | (map reduceMax (windows (2, 1) (2, 1))
7 | (map reduceMax (windows (2, 1) (2, 1))
8 | (map flatten (windows (4, 4) (2, 2) T))
9 | ))))))) S)
```

Then the IR-accelerator rules above rewrite each of these four map reduceMax instances to the FlexASR fragment. The listings for this example are in Figure 7 of Appendix C, with the result of applying the IR-accelerator mapping in part (d).

Note that each of the map reduceMax instances in the rewritten IR program is mapped to a composition of three FlexASR instructions (as shown in the IR-accelerator mapping rewrite rule), where fasrMaxpStore stores the input data into FlexASR, fasrMaxPool performs the maxpool computation in FlexASR, and fasrMaxpLoad loads the output result from FlexASR. When four of these instances are composed, the initial store and the final load are needed to communicate with FlexASR; however, the other intermediate transfers can be eliminated, since the output of one instance serves as input of another. We plan to enhance our prototype to cancel such redundant transfers, with the final optimized result shown in part (f) of Figure 7 in Appendix C.

This example illustrates the importance of minimizing data transfers while offloading operations to accelerators. Note that a fixed set of accelerator APIs may not allow such

[†] Average simulation time of running one data point (e.g., an image or a sentence) on a 2.4GHz AMD EPYC 7532 core.

optimizations, whereas D2A provides this flexibility through individual accelerator instructions. In future work, we would like to consider more general optimizations on the accelerator side that account for memory organization and data movement, potentially leveraging standard register allocation as well as recent DL operator fusion techniques [54].

5.2 Extending Formal Verification of Mappings

In our study (§ 4.4.1), we explored CHC-based verification of IR-accelerator mappings for fixed-size tensors (with symbolic data) and supplied relational loop invariants to the verifier. In future work, we would like to add support for symbolic-sized tensors and automatic inference of relational loop invariants. Additionally, our simulation validation reveals that custom numerics can significantly impact model accuracy. We would like to extend our verification to account for custom numerics and check or derive error bounds.

6 Related Work

The key insight of the D2A methodology is using the ILA as a formal software/hardware interface for mapping DSL applications to specialized accelerators. Below we survey past work on different aspects of D2A's features.

6.1 Software/Hardware Co-design

Recent work on accelerator generation and integration [4, 76] has explored adding support in the Halide [59] compiler flow for specialized Coarse-Grained Reconfigurable Array (CGRA) accelerators. That work composes an impressive array of custom tools to generate and verify specialized CGRA accelerators and also map Halide program fragments down to accelerator invocations. HeteroCL [42] also provides a similar custom flow. In contrast, the D2A methodology is designed to support software/hardware co-design by mitigating impedance mismatches between the granularity of *independently developed* DSLs and *near-arbitrary* accelerators; because of the flexibility of the ILA, the D2A methodology is applicable to a broader class of compilers and accelerators.

6.2 Pattern Matching Accelerator Calls

In principle, many DSLs allow for supporting custom accelerators via bespoke translations from DSL operators to specific accelerator APIs, e.g., as in the original TVM [14] support for VTA [50]. TVM's BYOC [16] interface eases incorporating custom accelerators by performing syntactic pattern matching to offload computations via user-provided code generators. However, BYOC leaves all matters of code generation, e.g., MMIO invocations, to the user, while D2A provides more structure to code generation via the ILA. In particular, the ILA provides useful simulation and verification capabilities. Additionally, BYOC's pattern matching cannot search the space of programs equivalent to the input, limiting the

number of potential accelerator invocations compared to flexible matching in our D2A prototype.

The MLIR framework [44] provides a rich metalanguage and numerous tools for developing, optimizing, and translating between custom compiler IRs, but does not inherently provide direct support for D2A's features. It would be possible to realize the D2A methodology within an MLIR-based ecosystem; we implemented our DL-focused prototype using TVM since it allowed leveraging more DL infrastructure.

Past work has also explored rewrite-based techniques for automatically inferring instruction selection passes between ISAs [60]. Rewriting in D2A instead operates on a highlevel DSL to expose opportunities to invoke code generators, rather than performing low-level code generation directly.

6.3 Validating and Verifying Accelerator Calls

Tools like Verilator [78] and Cuttlesim [58] enable efficient RTL-level simulation, but do not provide reusable interfaces or flexible matching to incorporate custom accelerators into existing compiler flows. Formally verified compilers such as CompCert [45] and CakeML [41] can rigorously establish end-to-end equivalence from high-level source code down to assembly for various CPU back-ends via machine-checkable proofs, but currently do not provide a general approach for integrating new accelerator support and provide no support for custom numerics. In contrast, D2A enables validating accelerator mappings via end-to-end simulation handling custom numerics and formally verifying individual rewrite rules from compiler IR patterns to accelerator invocations.

7 Conclusions

In this work we address key gaps preventing effective accelerator utilization under the prevalent API-based approach. Specifically, we highlight the lack of portability, the inability to integrate accelerators into optimizing compilers, and the inability to validate generated code. We show that the root of these gaps is the lack of a formal software/hardware interface for accelerators, and use the recently developed ILA specification for this purpose in our proposed D2A methodology. We describe a D2A prototype for DL applications using the TVM and ILAng frameworks. We evaluate the capabilities of this prototype through the fully automated compilation of six applications on three different accelerator platforms. We show the convenience of equality saturation-based flexible matching by mapping of a larger set of accelerator-supported operations in DSL applications than is possible using exact matching. We also discuss case studies that highlight the ability to (a) formally verify the equivalence of compiler IR to accelerator mappings of individual accelerator operations (using abstract data types) and (b) do automated applicationlevel simulation-based validation using the accelerator numerics to check the acceptability of application-level results even with deviations at the operation level due to numerics. The latter exposed precision issues in various case studies which required modification of the accelerator numerics, demonstrating its use in software/hardware co-design. Other than the device ILAs, integration into the compiler required only a small number of Glenside rewrite rules and a small code generator mapping matched patterns to ILA instructions. We believe this is the first compiler framework that addresses the multiple issues in effective accelerator utilization and establishes a foundation that can democratize the end-to-end mapping of applications in DSLs to accelerator-rich platforms, no longer limiting it to large enterprises that can afford teams of hardware, software, and system experts.

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Appendix A Supported Accelerator Operations

For each of the accelerators discussed in § 4.1, our prototype compiler supports specific operations through the compiler-IR accelerator mappings.

FlexASR. The compiler supports two of FlexASR's operations: linear layers (illustrated in Figure 5) and LSTM layers. For simplicity, the pattern we match for the LSTM layer in exact matching is precisely the formulation of an LSTM produced by TVM's PyTorch importer, which is "unrolled" to the correct number of timesteps (35 in the case of our LSTM-WLM application). For flexible matching, we translate the "unrolled" LSTM in Relay into Glenside and also match it in the target Glenside program. In principle, it would be possible to define a rewrite rule corresponding to a single LSTM timestep, and another rewrite to "fold" adjacent timesteps into a single FlexASR LSTM layer invocation (one ILA instruction) with the total number of timesteps.

HLSCNN. Our HLSCNN specification has only one operation, a non-grouped 2D convolution. In Relay and Glenside, we map any non-grouped 2D convolution (nn.conv2d) to the HLSCNN convolution operation. Note that the Relay convolution operation allows for padding an input before convolving it; our implementation pads on the host before invoking the accelerator. In principle, it would be possible to rewrite a grouped convolution into a concatenation of non-grouped convolutions, but the number of groups in the models in § 4.2 tended to be large (960 groups in MobileNet), which would blow up the programs and be impractical to run on a single device.

VTA. Unlike the above accelerators, VTA is a fine-grained programmable accelerator with a defined ISA. Hence, "operators" in VTA are really sequences of VTA instructions that implement the semantics of a tensor operator in Relay. TVM has a built-in bespoke code generator for VTA, which operates on TVM's lower-level Halide-like DSL and directly implements arbitrary tensor operations for VTA. In principle, it would be possible for us to adapt the existing VTA code generator to instead output VTA ILA instructions, resembling traditional instruction selection. For simplicity, our prototype implements matrix multiplication and addition as fixed sequences of VTA ILA instructions.

Appendix B Application Parameters

We provide further details for the applications listed in § 4.2.

• EfficientNet: We used a publicly available implementation of EfficientNet⁵ in MxNet, pretrained on ImageNet (image size 224 × 224, with 1000 classes). We imported it through TVM's MxNet importer.

- LSTM-WLM: We used the LSTM model implementation from the official PyTorch examples repository,6 training on WikiText-2 with the provided script on the following settings: 40 epochs, a batch size of 20, sequence length of 35, and an initial learning rate of 20, with a single layer for the LSTM. We imported it through TVM's PyTorch importer with one simplification in the importer: for simplicity, our FlexASR LSTM layer integration only returned the LSTM's sequence output but not the final hidden and cell states (even though the device itself supports this). In order to match the semantics between our integration and the LSTM, we modified the imported LSTM not to return the final hidden and cell states either. In future work, it would be feasible for us to support returning the final hidden and cell states and eliminate this simplification.
- **MobileNet V2**: We used an open-source implementation of MobileNetV2⁷ in PyTorch and used the implementation's provided script to train on CIFAR-10, training for 200 epochs with a learning rate of 0.01 and a batch size of 128. We imported it using TVM's PyTorch importer.
- **ResMLP**: We used an open-source ResMLP implementation⁸ in PyTorch. We used similar parameters as those reported in [75] for training on CIFAR: 384 features, 12 layers, and a patch size of 16. We trained it on CIFAR-10 for 100 epochs with a learning rate of 0.01, though in Table 4, we note that we obtained a lower reference accuracy on CIFAR-10 than that reported in [75]. We are not certain that we trained using all the same settings as in the original work and (in order to reduce the load on the simulator) we trained and evaluated on 32×32 images, whereas the original work scaled the images up to 256 × 256. We imported the model through TVM's PyTorch importer.
- ResNet-20: We used the Gluon Model Zoo's implementation of ResNet-20 in MxNet,⁹ pretrained on CIFAR-10. We imported it unmodified through TVM's MxNet importer.
- Transformer: We used the nn.Transformer implementation from PyTorch, with 8 heads, 6 encoder layers, 6 decoder layers, and 256 features (left untrained). These settings were based on a TVM PyTorch importer unit test.

Appendix C Illustrative Code Fragments

The figures below provide examples of ILA fragments and various rewrites at greater length.

⁵https://github.com/mnikitin/EfficientNet, accessed Nov. 18, 2021.

⁶https://github.com/pytorch/examples/tree/master/word_language_model, accessed Nov. 18, 2021.

⁷https://github.com/kuangliu/pytorch-cifar, accessed Nov. 18, 2021.

⁸https://github.com/lucidrains/res-mlp-pytorch, accessed Nov. 18, 2021.

https://cv.gluon.ai/api/model_zoo.html#gluoncv.model_zoo.cifar_resnet20 v1, accessed Nov. 18, 2021.

(a) Compiler IR instructions

```
1 | ComILA.relay_nn_dense
2 | ComILA.relay_bias_add
                                             (b) Compiler IR ILA program fragment
    // 1. writing data into the accelerator memory
    FlexASR_ILA.write_v
3
    // 2. configuring the accelerator for executing linear layer operation
4
   FlexASR_ILA.pe_cfg_rnn_layer_sizing
5
   FlexASR_ILA.pe_cfg_mngr
    FlexASR_ILA.pe_cfg_act_mngr
   FlexASR_ILA.pe_cfg_act_v
8
   FlexASR_ILA.gb_cfg_mmngr_gb_large
    FlexASR_ILA.gb_cfg_gb_control
10
11
    // 3. triggering the accelerator linear function
12
   FlexASR_ILA.fn_start
    // 4. reading data out from the accelerator memory (if needed)
13
14
    FlexASR_ILA.read_v
15 I
                                               (c) FlexASR ILA program fragment
1
    // 1. writing data into the accelerator memory
2
    Write, addr=0xA4500000, data=0x0F0EFFBF8F746F9FB58D148E0EB7BFDAD
    // 2. configurating the accelerator states for linear layer operation
4
    Write, addr=0xA4400010, data=0x0010101000001
5
    Write, addr=0xA4400020, data=0x0000000010000000102020200
6
7
    Write, addr=0xA4800010, data=0x000000000102050001
8
    // 3. triggering the accelerator function
9
    Write, addr=0xA3000010, data=0x1
11
    // 4. reading data out from the accelerator memory (if needed)
12
    Read, addr=0xA3500200, data=0x0
13 | ...
```

(d) FlexASR MMIO commands

Figure 5. IR-accelerator mapping for the FlexASR LinearLayer operation. This shows a many-to-many mapping from Relay IR instructions to a sequence of FlexASR MMIO commands. (a) LinearLayer in Relay consists of a linear transformation operation nn. dense, followed by a bias addition operation nn. bias_add. (b) The compiler IR ILA instruction has an one-to-one mapping to the compiler IR instruction. (c) The FlexASR ILA program fragment in its assembly format: It includes: (1) write instructions to transfer the data into FlexASR's memory. (2) setting up FlexASR LinearLayer configuration states, for example, the instruction at line 5 sets the states of FlexASR layer sizing information. (3) instruction that triggers the FlexASR LinearLayer computation (5) read data out from FlexASR's memory if needed. (d) The MMIO commands for FlexASR have a one-to-one mapping to its FlexASR ILA instructions.

```
#include <ilang/ilang++.h>
1
     int main() {
     // declare an ILA model module
4
5
     auto m = ilang::Ila("flexasr-ila");
6
7
    // declare model interface input ports
     m.NewBvInput("top_if_wr", TOP_IF_WR_BITWIDTH);
8
    m.NewBvInput("top_if_rd", TOP_IF_RD_BITWIDTH);
9
10
     m.NewBvInput("top_addr_in", TOP_ADDR_IN_BITWIDTH);
11
     m.NewBvInput("top_data_in", TOP_DATA_IN_BITWIDTH);
12
    // declare architectural states
13
     m.NewBvState("pe_0_is_valid", PE_VALID_BITWIDTH);
14
15
     m.NewBvState("pe_0_is_bias", PE_IS_BIAS_BITWIDTH);
16
17
     m.NewMemState("gb_large_buffer", TOP_ADDR_IN_BITWIDTH, TOP_DATA_IN_BITWIDTH);
18
     // define ILA instructions
19
20
    { // ILA instruction for configuring pe_cfg_mngr
21
     auto instr = m.NewInstr("pe_0_cfg_mngr");
22
     \ensuremath{//} define decode condition for this instruction
23
     auto is_write = (m.input("top_if_wr") == 1) & (m.input("top_if_rd") == 0);
24
25
    instr.SetDecode(is_write & (m.input("top_addr_in") == PE_0_CFG_MNGR_ADDR));
26
    // define state update functions for this instruction
27
    auto is_valid = ilang::SelectBit(m.input("top_data_in"), PE_IS_VALID_BIT_IDX);
28
    instr.SetUpdate(m.state("pe_0_is_valid"), is_valid);
29
    auto is_bias = ilang::SelectBit(m.input("top_data_in"), PE_IS_BIAS_BIT_IDX);
30
31
     instr.SetUpdate(m.state("pe_0_is_bias"), is_bias);
32
33
34
    // other ILA instructions
35
```

Figure 6. FlexASR ILA model snippet. Lines 5-18 define the FlexASR ILA model, its input and architectural states variables. Lines 20-32 shows an example of an ILA instruction named "pe_0_cfg_mngr," which corresponds to line 6 in Figure 5 (c). In each ILA instruction, we specify its decode condition and state update functions. For example, in this instruction, the decode condition (line 24-25) is when there is write instruction at the top interface to the address associated with the configuration of the PE's management configuration. Lines 27-32 show this instruction's state update functions for the architectural states. In this example, this ILA instruction models the behavior of storing the arguments from the input data at its interface into the FlexASR configuration registers. From this example, we can see that the ILA instructions provide an abstraction of the functionality of the accelerator corresponding to the MMIO instructions at its interface.

```
; (a) IR-accelerator rewrite rule for FlexASR's temporal max-pooling (which corresponds to
           ; 2D max-pooling with window shape and stride (2, 1))
           (map reduceMax (windows (2, 1) (2, 1) ?T)) -> (fasrMaxpLoad (fasrMaxpool (fasrMaxpStore ?T)))
 4
 5
           ; (b) Initial Glenside program for a 2D max-pooling layer with window shape (4,\ 4)
 6
           ; and stride (2, 2). We use T to denote the input of the 2D max-pooling layer.
           (map reduceMax (windows (4, 4) (2, 2) T))
           ; (c) A rewritten IR program found via Glenside
 9
10
           ; T denotes the input of the 2D max-pooling layer, and S is the shape of the output of the 2D max-pooling layer
11
           (reshape (map reduceMax (windows (2, 1) (2, 1)
12
           (map reduceMax (windows (2, 1) (2, 1)
           (map reduceMax (windows (2, 1) (2, 1)
           (map reduceMax (windows (2, 1) (2, 1)
14
15
           (map flatten (windows (4, 4) (2, 2) T)) )))))))))))))))
16
17
           ; (d) 2D max-pooling using FlexASR
18
           (reshape (fasrMaxpLoad (fasrMaxpool (fasrMaxpStore
           (fasrMaxpLoad (fasrMaxpool (fasrMaxpStore
19
20
          (fasrMaxpLoad (fasrMaxpool (fasrMaxpStore
21
          (fasrMaxpLoad (fasrMaxpool (fasrMaxpStore
22
          (map flatten (windows (4, 4) (2, 2) T)) )))))))))))))))))))))
23
24
          : (e) IR-accelerator rewrite rule to remove redundant Store-Loads
25
            ; Loading data out of the accelerator only to store it back to the same location is unnecessary
26
          (fasrMaxpStore (fasrMaxpLoad ?T) -> ?T
27
           ; (f) Optimized 2D max-pooling using FlexASR
28
          (reshape (fasrMaxpLoad (fasrMaxpool (fasrMaxpool (fasrMaxpool (fasrMaxpool (fasrMaxpload (fasrMaxplo
29
         (map flatten (windows (4, 4) (2, 2) T)) )))))) S)
```

Figure 7. How D2A offloads 2D max-pooling to FlexASR's temporal max-pooling operation. (a) The IR-accelerator rewrite rule for FlexASR's temporal max-pooling operation. (b) A Glenside program for a 2D max-pooling layer with window shape (4, 4) and stride (2, 2). Note that it does not contain a match for the left-hand side of the IR-accelerator rewrite rule. (c) An equivalent rewritten IR program found by flexible matching. It contains four instances of the left-hand side of the IR-accelerator rewrite rule. (d) A program offloading the 2D max-pooling layer to FlexASR produced by replacing each of the four instances with the right-hand side of the IR-accelerator rule. Note that in this program, the initial store and the final load are needed to communicate with FlexASR; however, the other intermediate loads/stores can be eliminated, since the output of one instance serves as input of another. (e) Another IR-accelerator rewrite rule that removes redundant Store-Loads. (f) An optimized program produced by applying the new rewrite rule. This program only performs a single (matrix) store at the start of the operation and a single (matrix) load to read the output at the end of the operation. In future, we hope to generalize this example and consider memory organization in accelerators and data-movement for optimizing data transfers.