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(45) **Date of Patent: Jun. 10, 2014**

(54) **VOLTAGE REGULATOR INTEGRATED WITH SEMICONDUCTOR CHIP**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 1163 days.

(21) Appl. No.: **11/964,015**

(22) Filed: **Dec. 25, 2007**

(65) **Prior Publication Data**

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Related U.S. Application Data

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(51) **Int. Cl.**

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H01L 27/11	(2006.01)
H01L 29/00	(2006.01)
H01L 23/58	(2006.01)
H01L 23/48	(2006.01)
H01L 23/52	(2006.01)
H01L 29/40	(2006.01)

(52) **U.S. Cl.**
USPC **257/531**; 257/379; 257/516; 257/528; 257/649; 257/738; 257/E27.033

(58) **Field of Classification Search**
None
See application file for complete search history.

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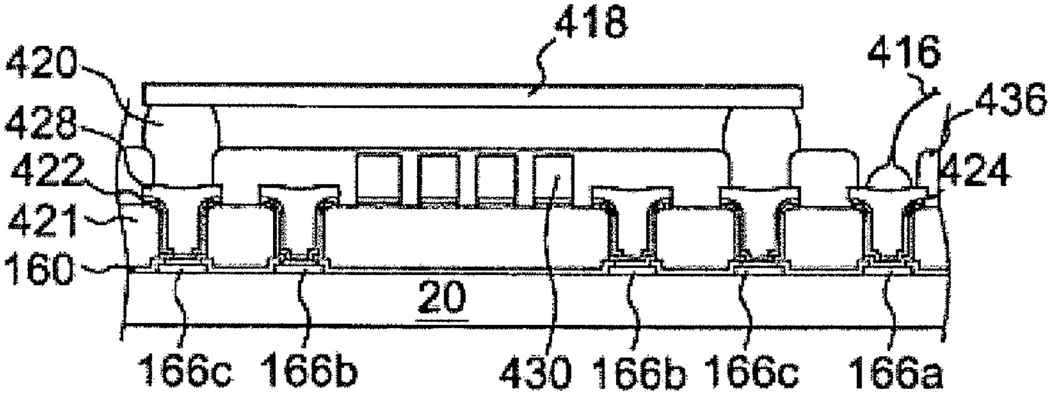
(74) *Attorney, Agent, or Firm* — Seyfarth Shaw LLP

(57) **ABSTRACT**

The present invention reveals a semiconductor chip structure and its application circuit network, wherein the switching voltage regulator or converter is integrated with a semiconductor chip by chip fabrication methods, so that the semiconductor chip has the ability to regulate voltage within a specific voltage range. Therefore, when many electrical devices of different working voltages are placed on a Printed Circuit Board (PCB), only a certain number of semiconductor chips need to be constructed. Originally, in order to account for the different demands in voltage, power supply units of different output voltages, or a variety of voltage regulators need to be added. However, using the built-in voltage regulator or converter, the voltage range can be immediately adjusted to that which is needed. This improvement allows for easier control of electrical devices of different working voltages and decreases response time of electrical devices.

20 Claims, 76 Drawing Sheets



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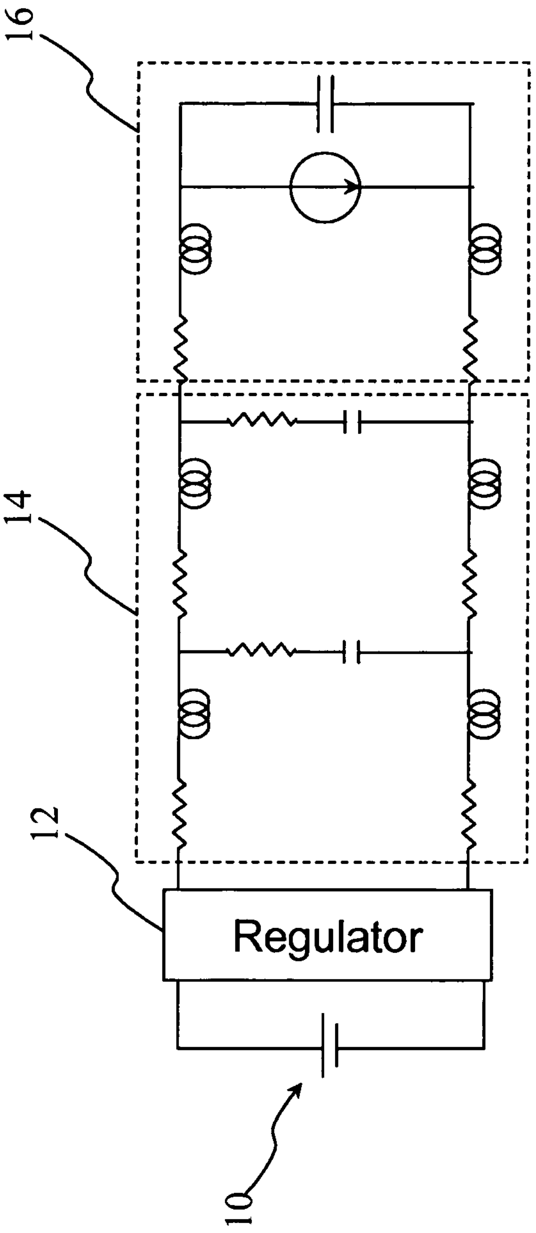

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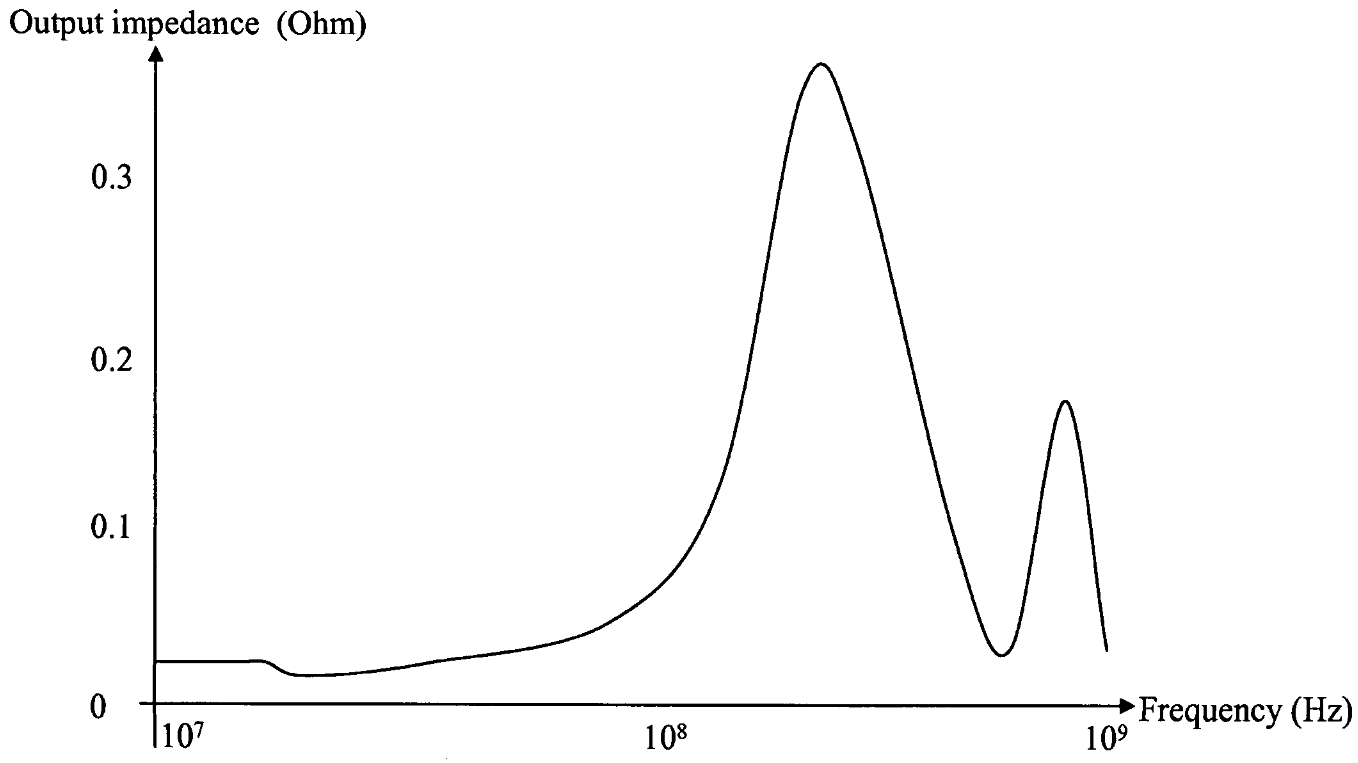

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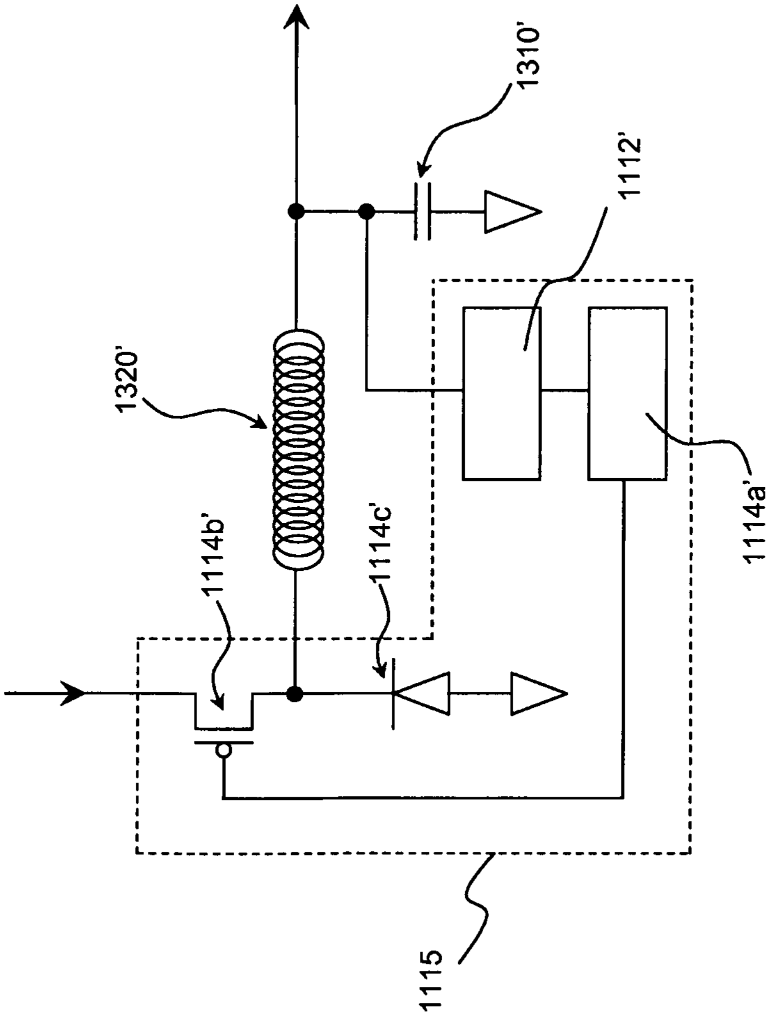


FIG. 3 (Prior Art)

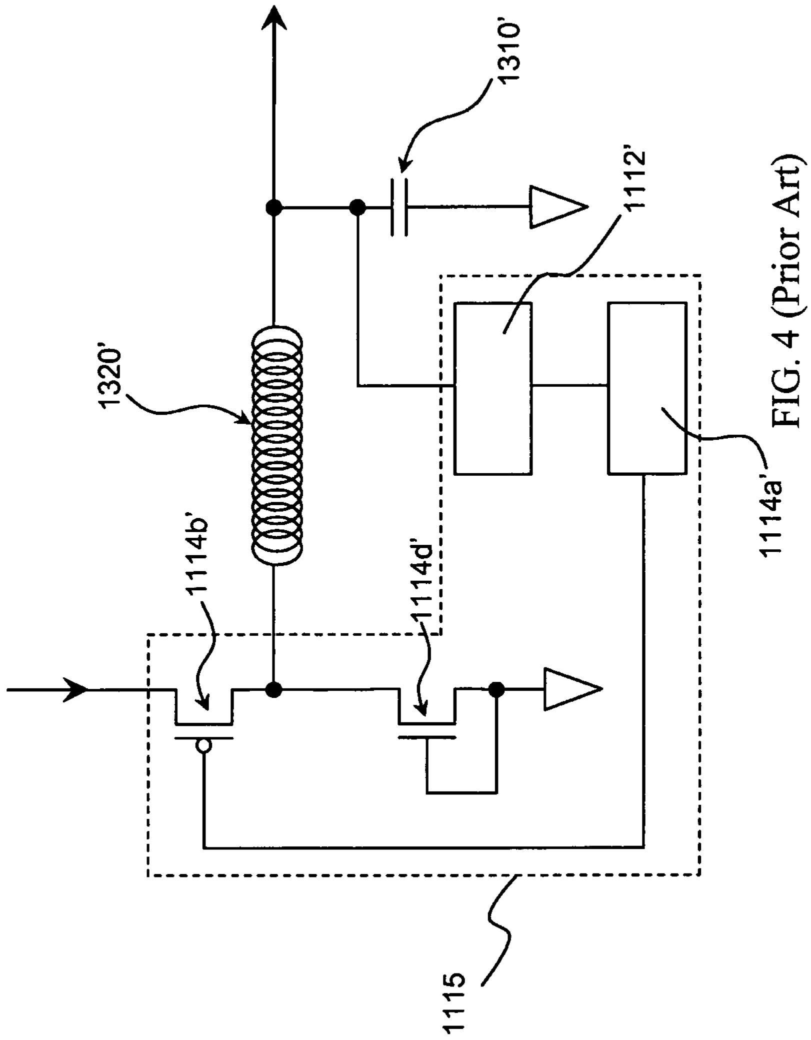
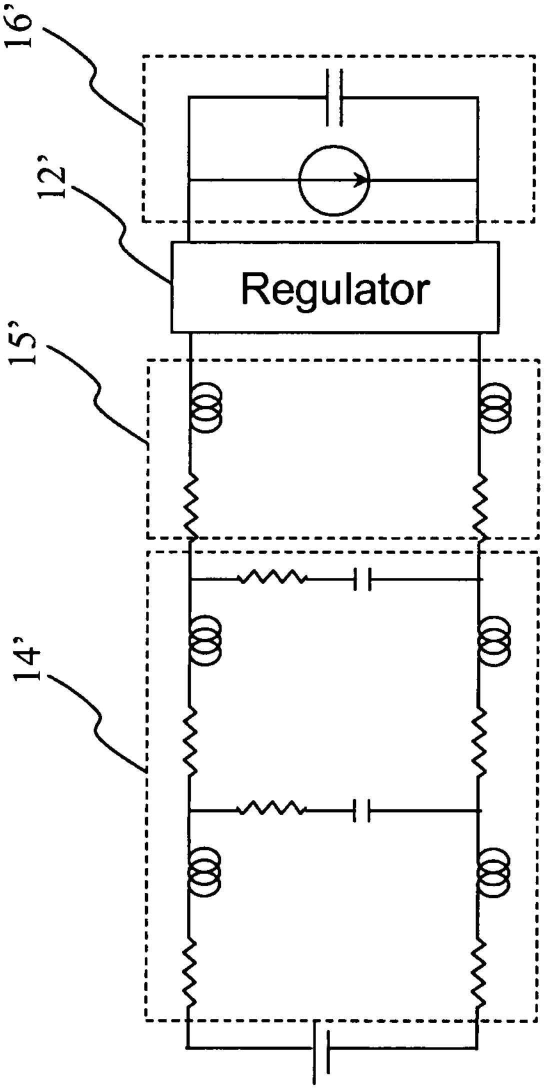


FIG. 4 (Prior Art)



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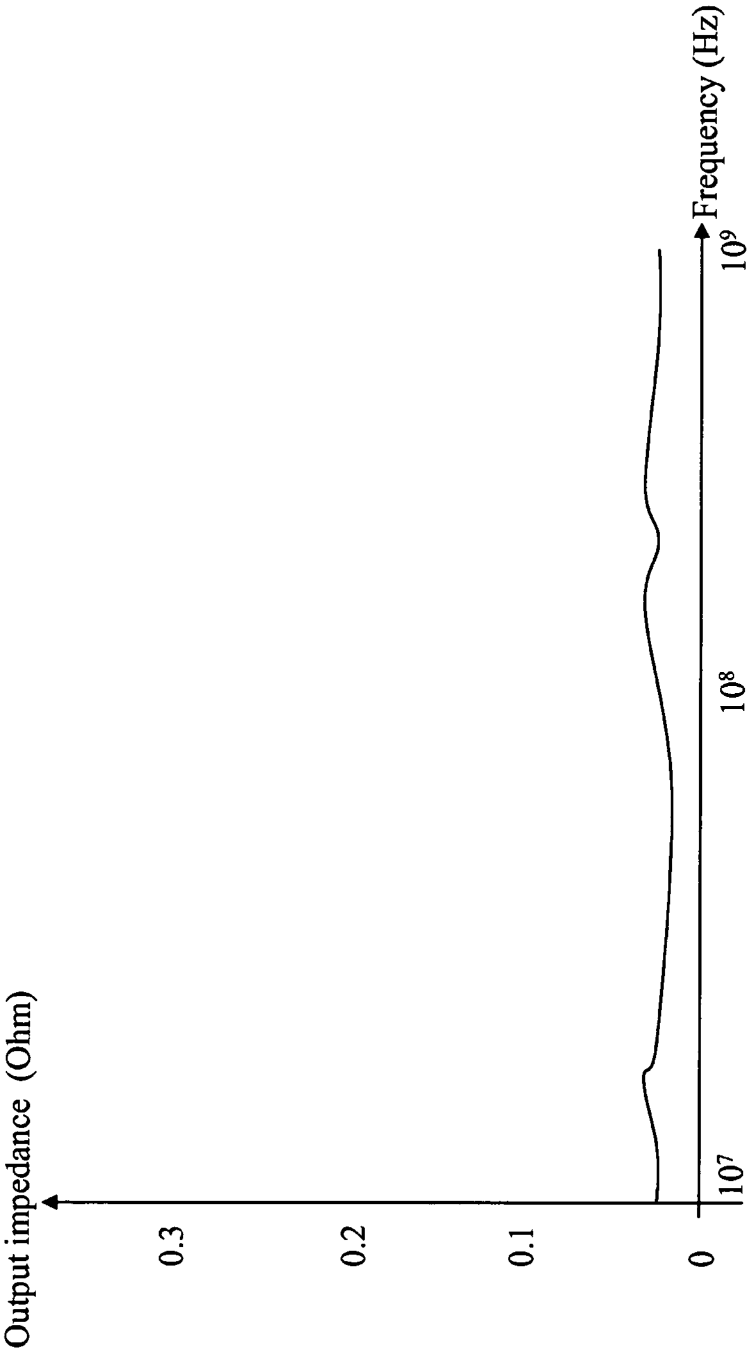

FIG. 6

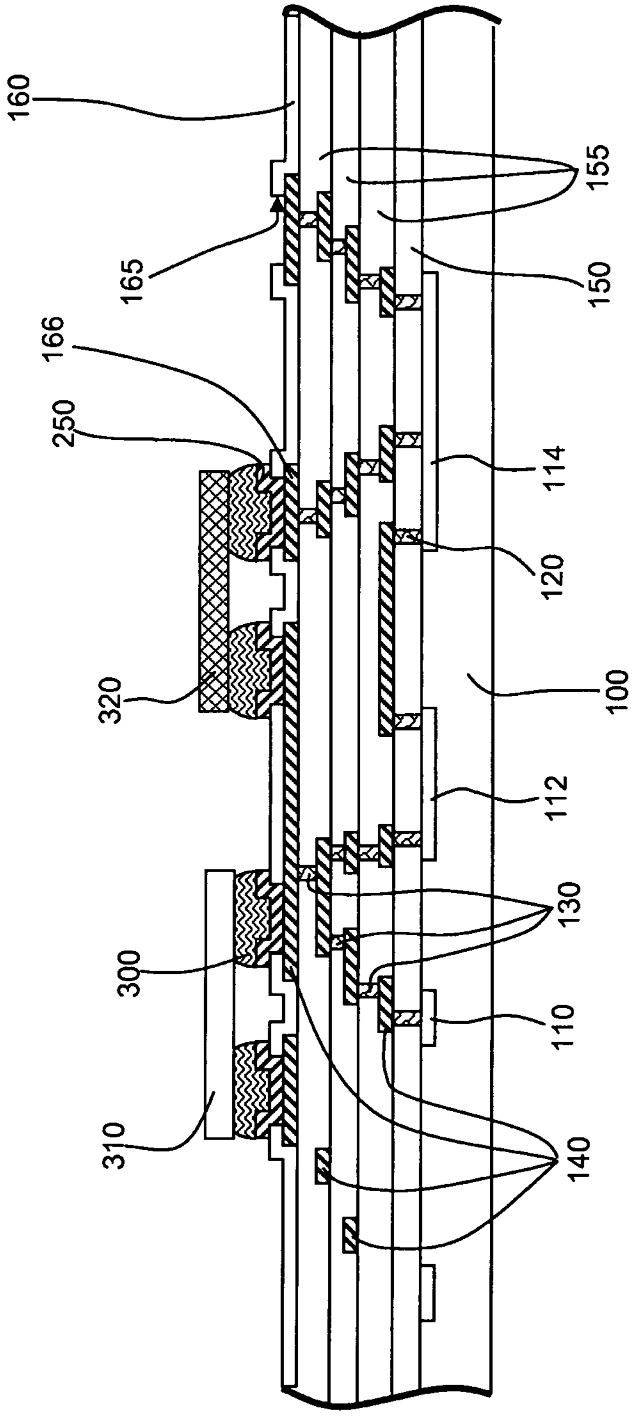

FIG. 7

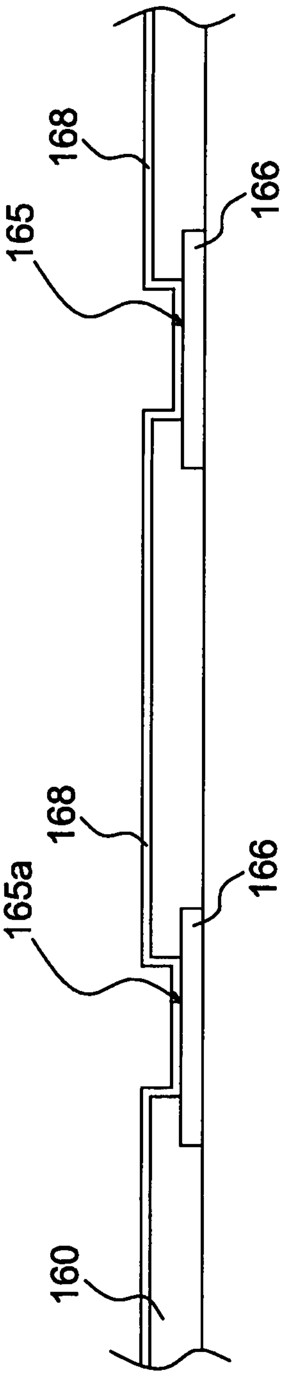

Fig. 7a

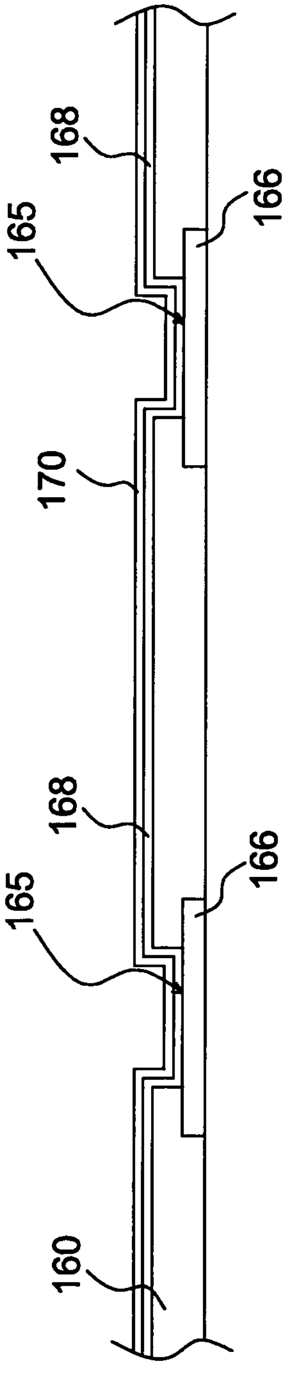

Fig. 7b

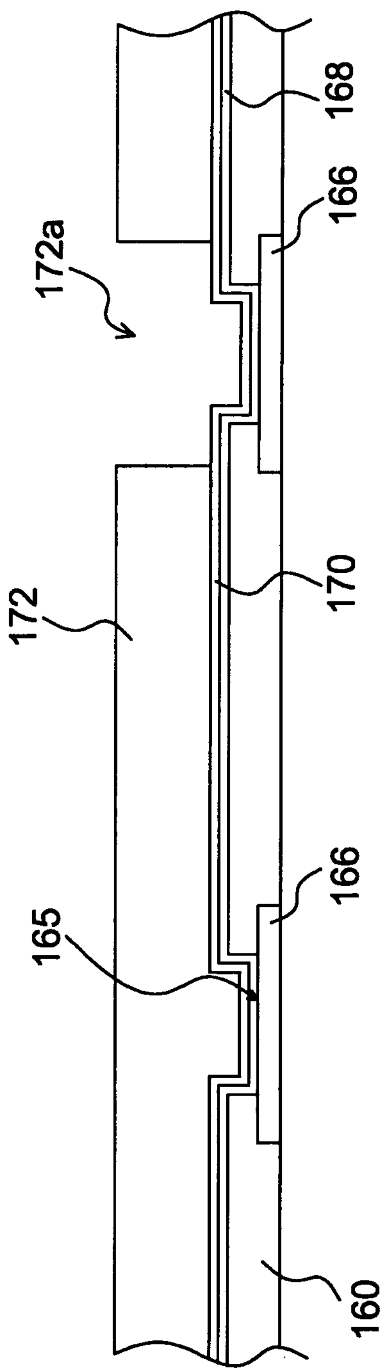
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Fig. 7c

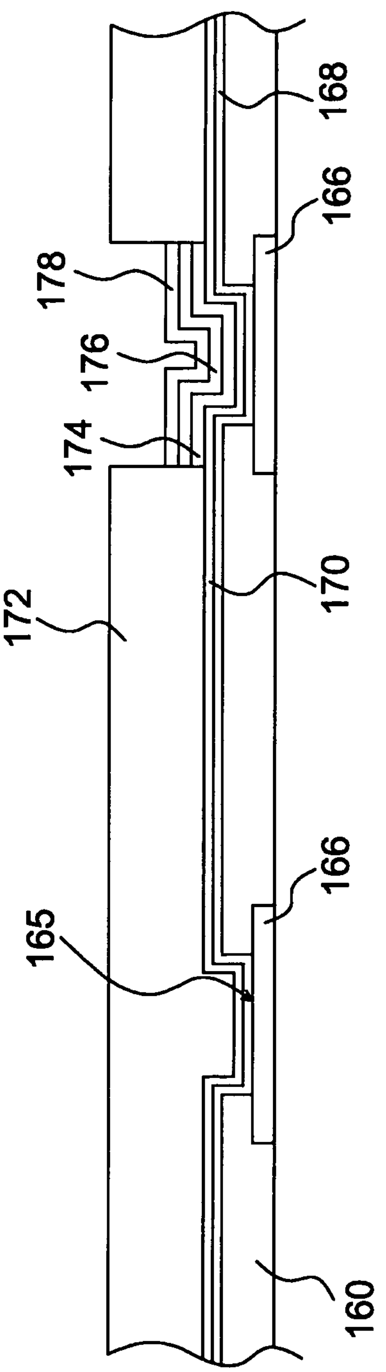
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Fig. 7d

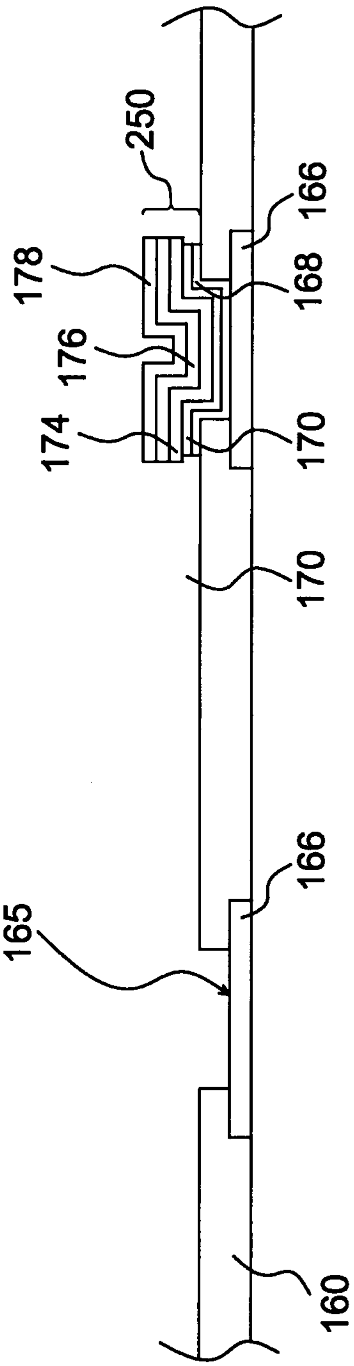

Fig. 7e

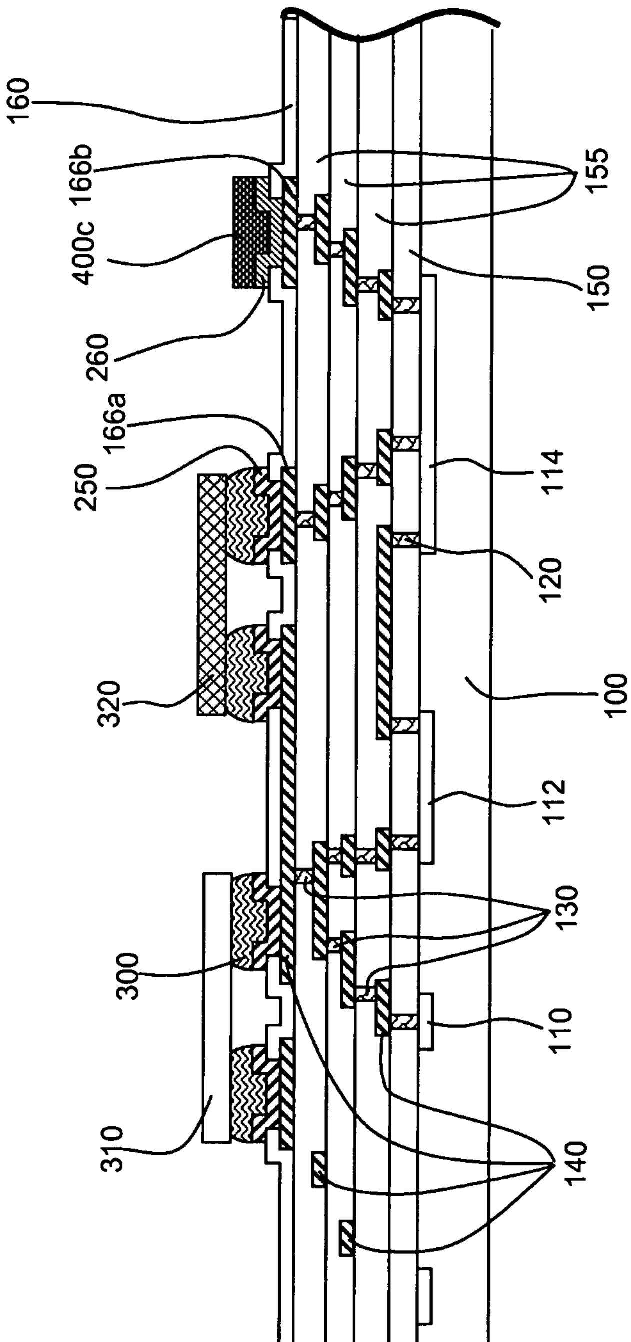
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FIG. 8

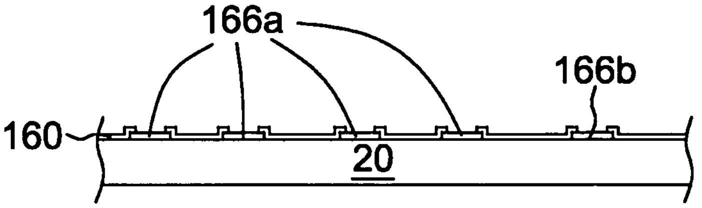


Fig. 8a

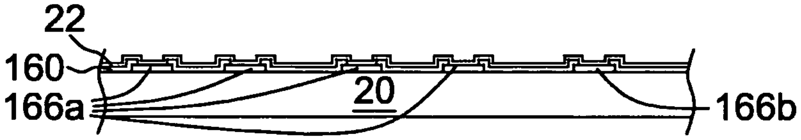


Fig. 8b

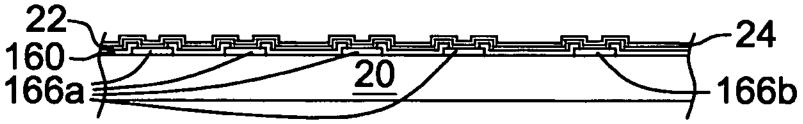


Fig. 8c

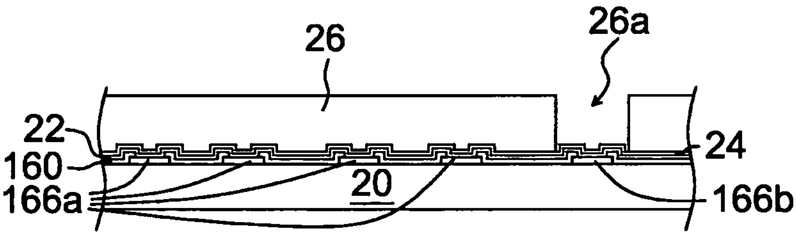


Fig. 8d

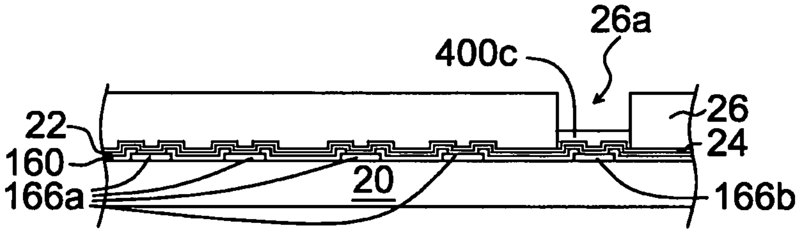
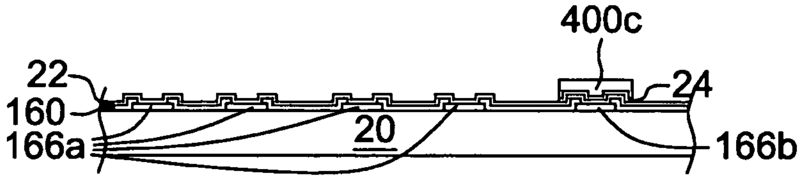


Fig. 8e



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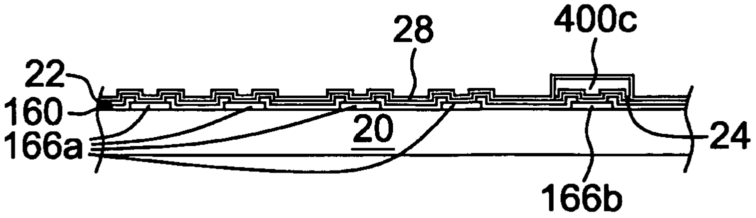

Fig. 8g

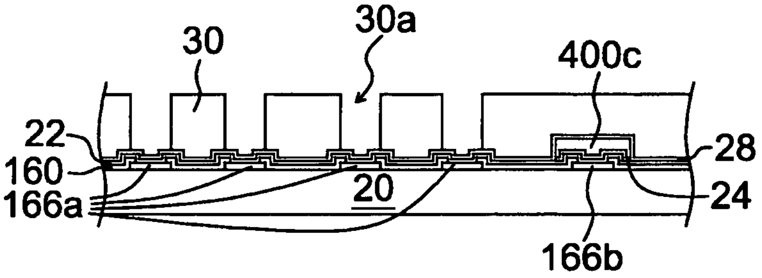

Fig. 8h

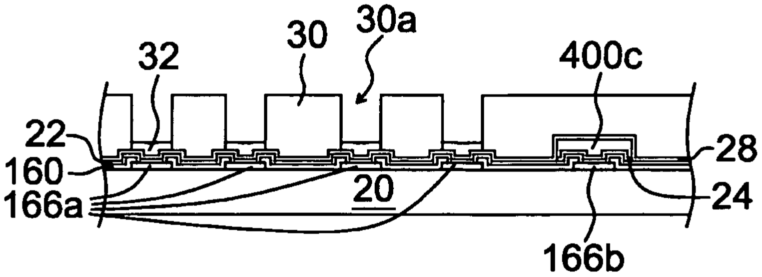

Fig. 8i

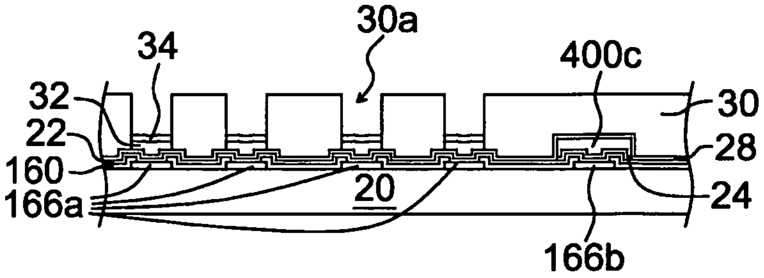

Fig. 8j

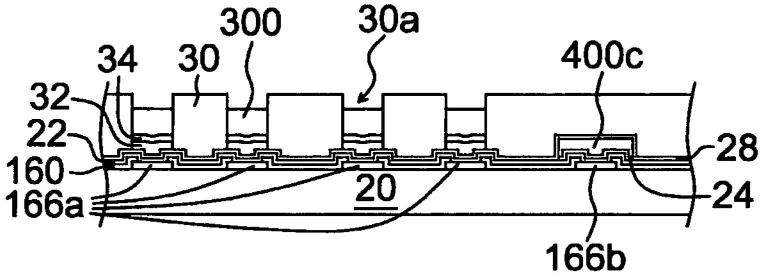

Fig. 8k

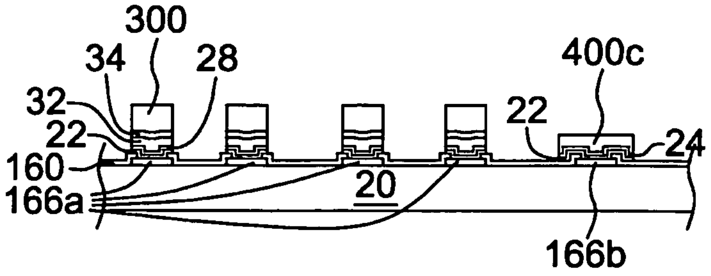

Fig. 8l

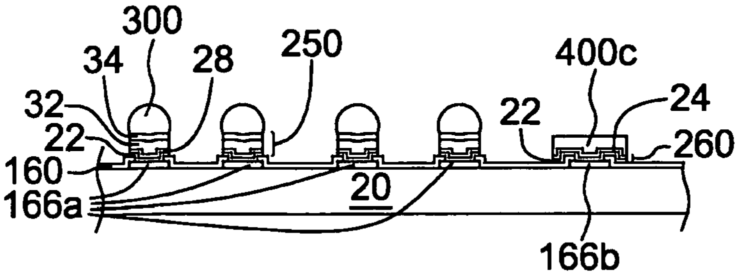

Fig. 8m

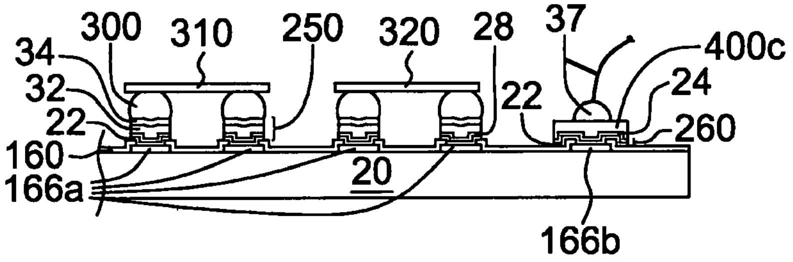

Fig. 8n

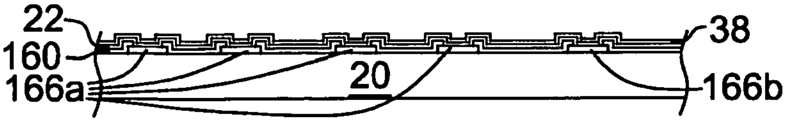

Fig. 8o

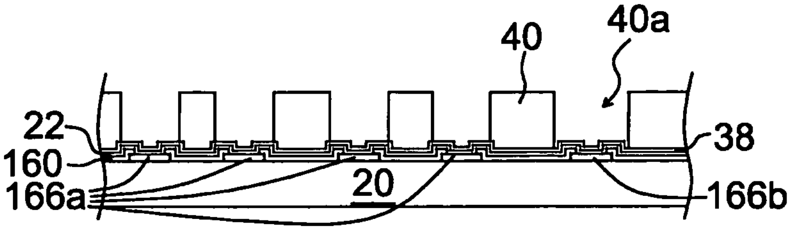

Fig. 8p

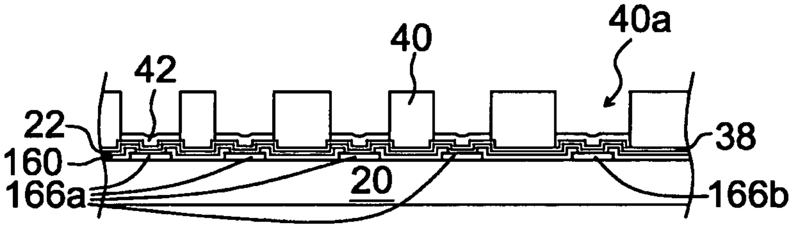

Fig. 8q

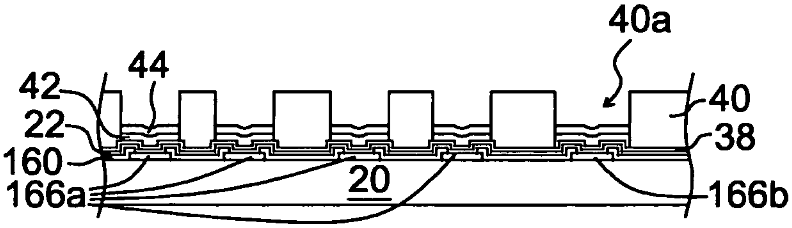

Fig. 8r

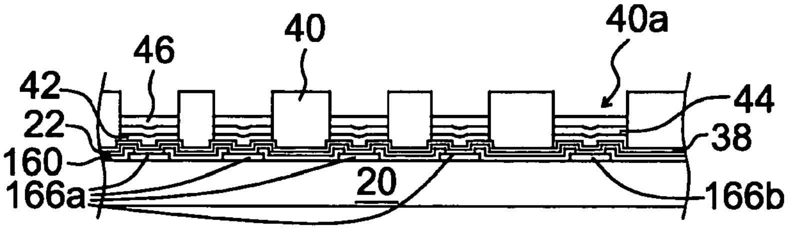

Fig. 8s

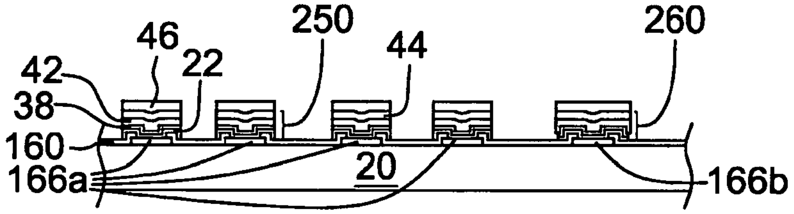

Fig. 8t

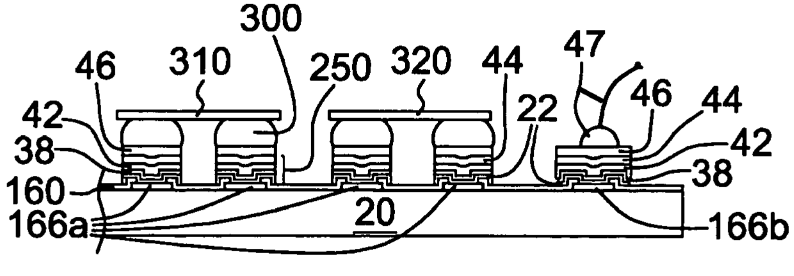

Fig. 8u

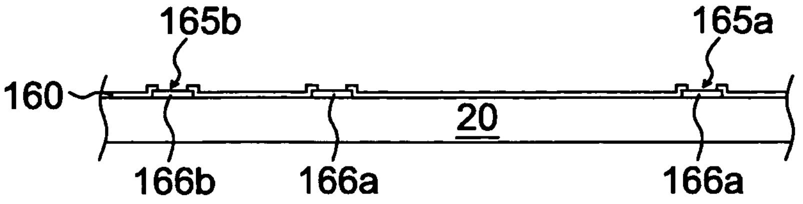

Fig.8aa

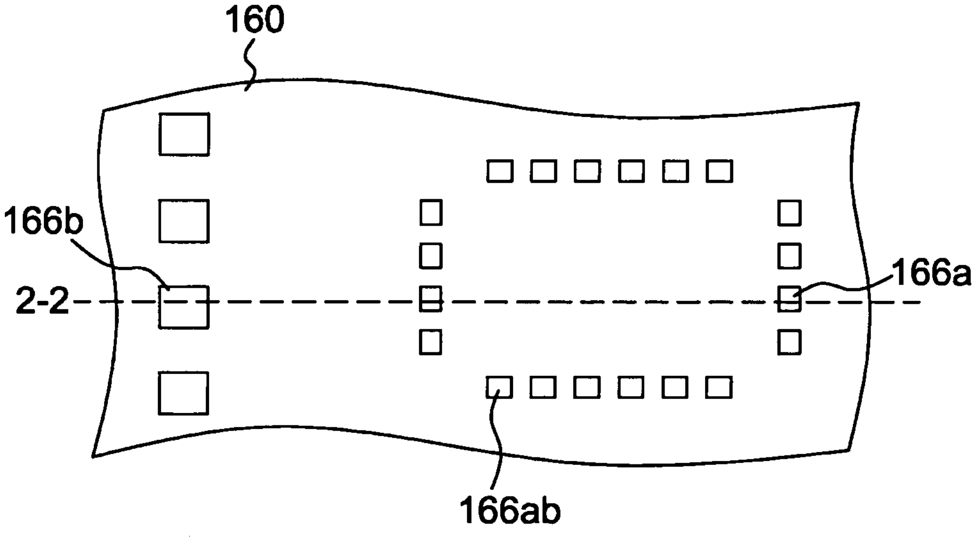

Fig.8ab

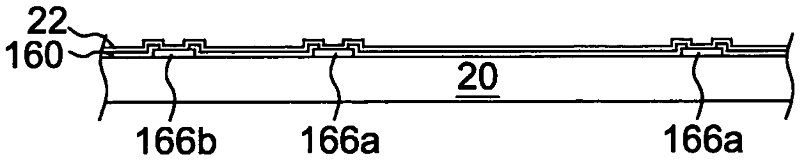

Fig.8ac

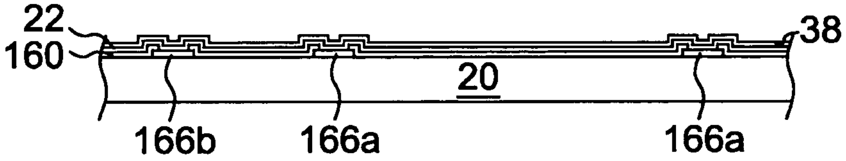

Fig.8ad

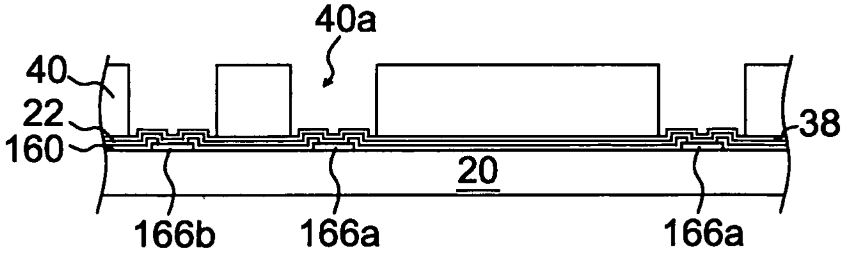

Fig.8ae

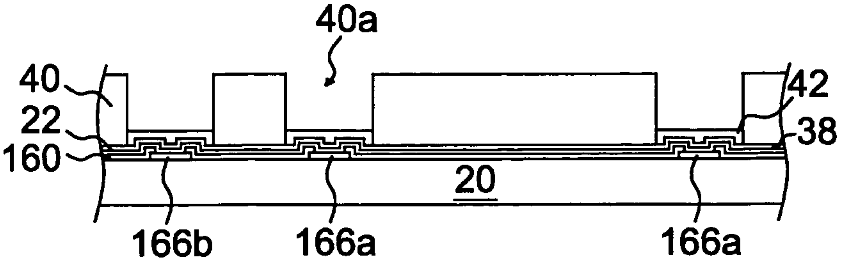

Fig.8af

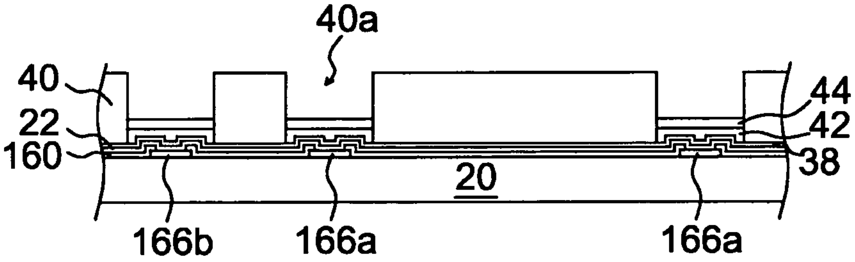

Fig.8ag

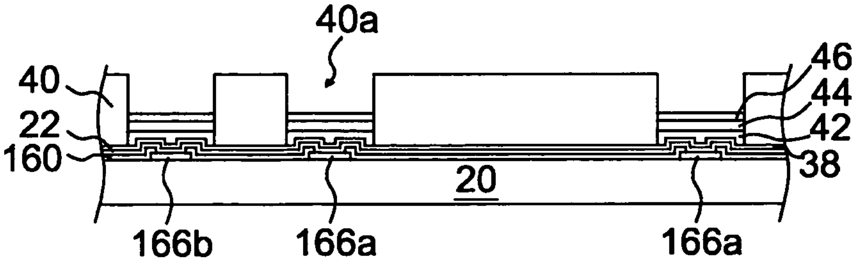

Fig.8ah

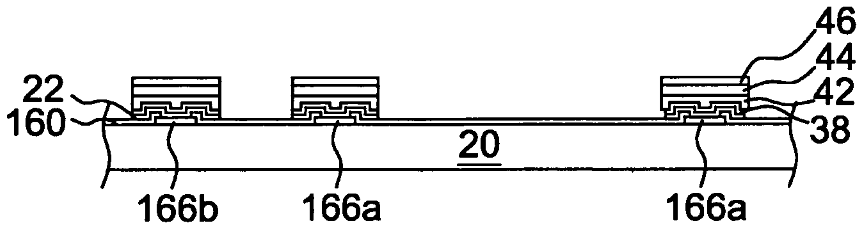

Fig.8ai

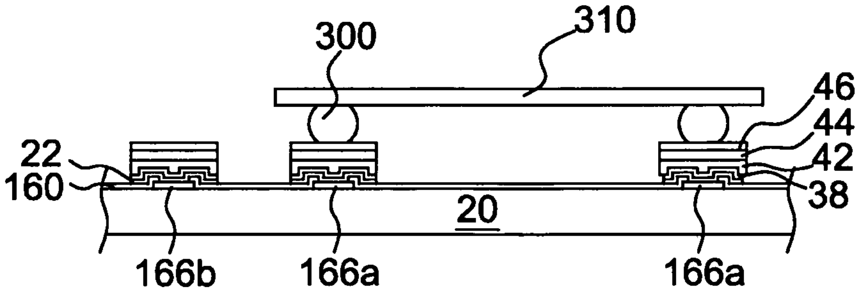

Fig.8aj

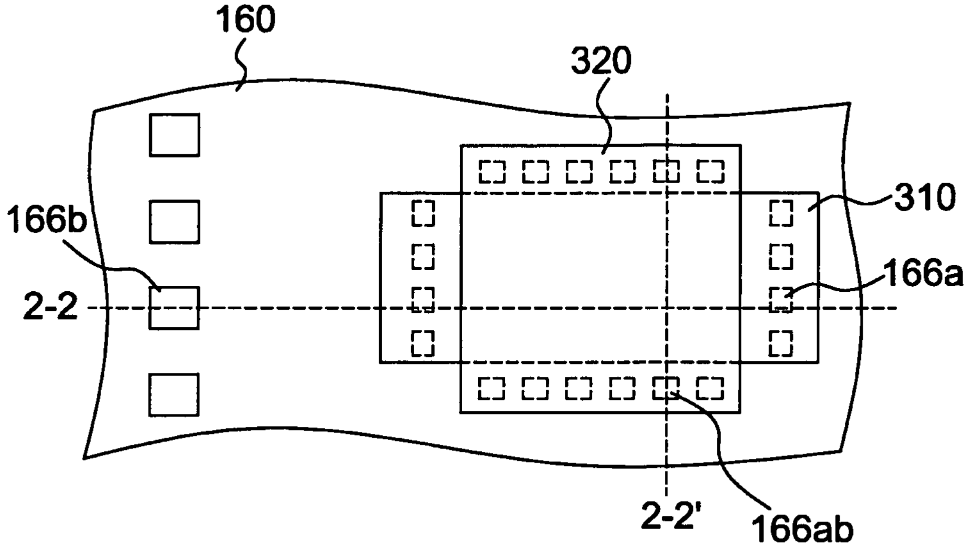

Fig.8ak

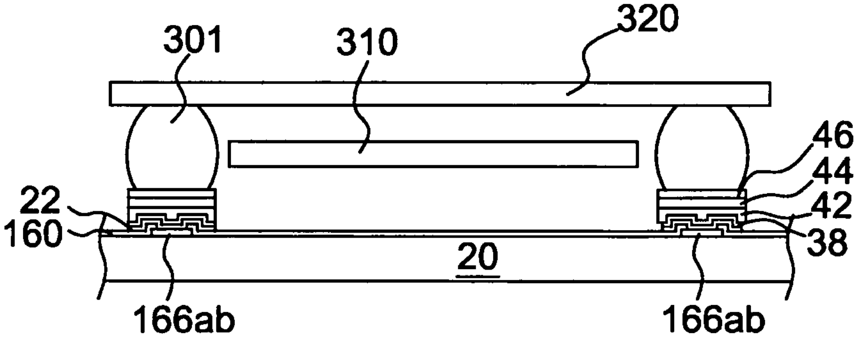

Fig.8al

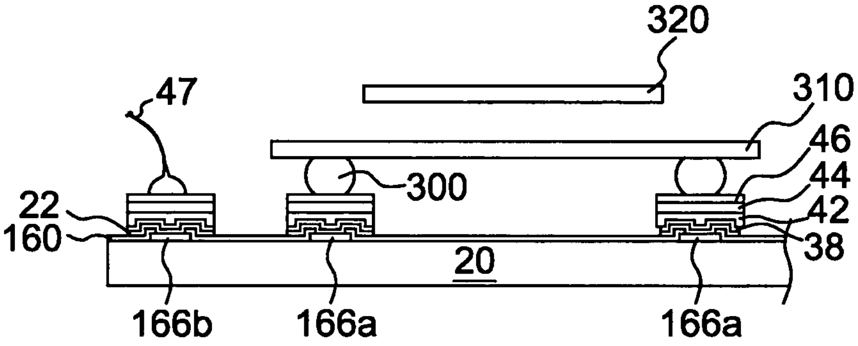

Fig.8am

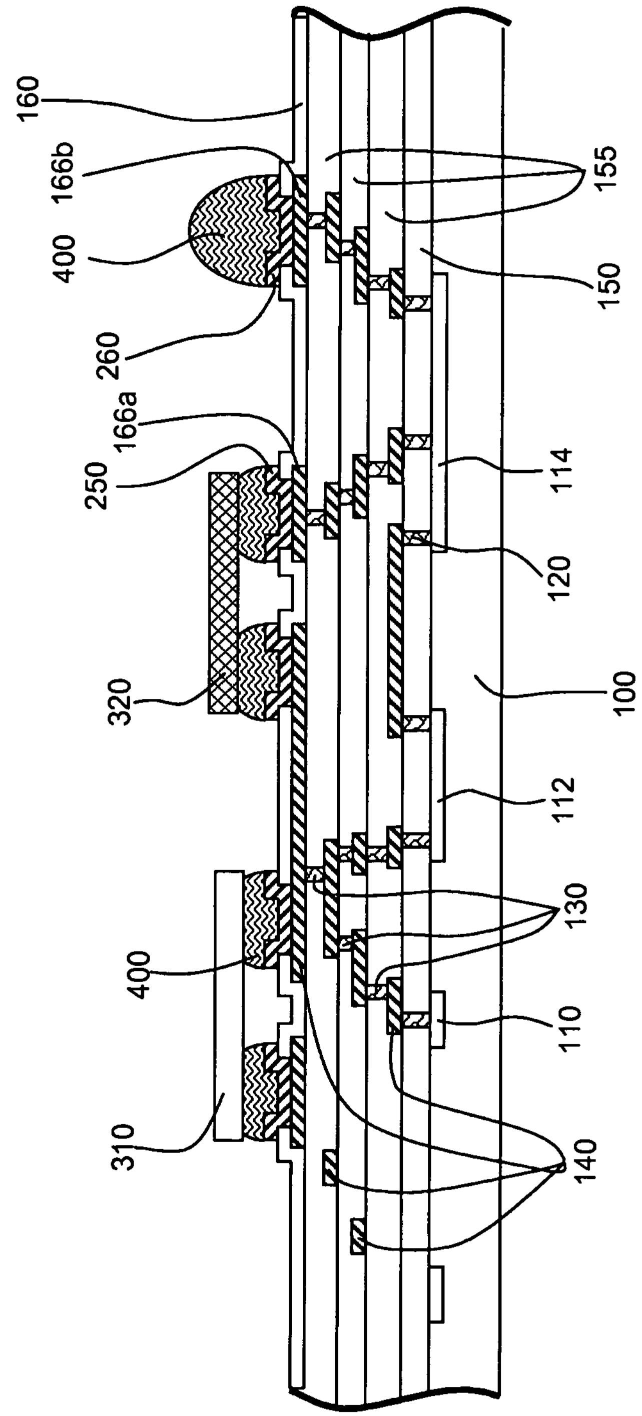
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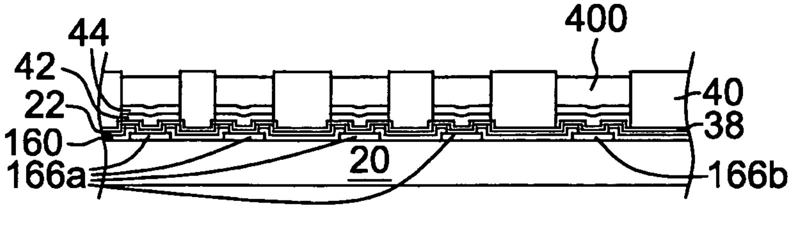
FIG. 9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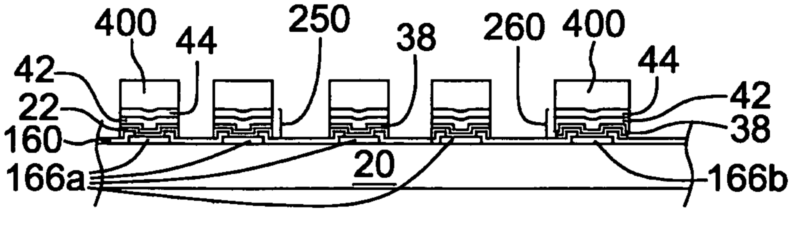
166b

Fig. 9a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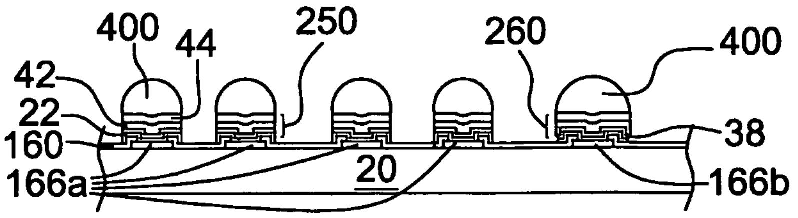
166b

Fig. 9b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166a
166b

Fig. 9c

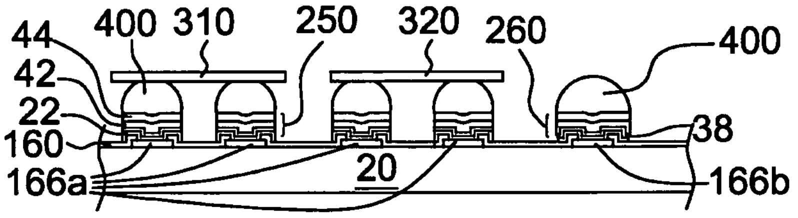
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Fig. 9d

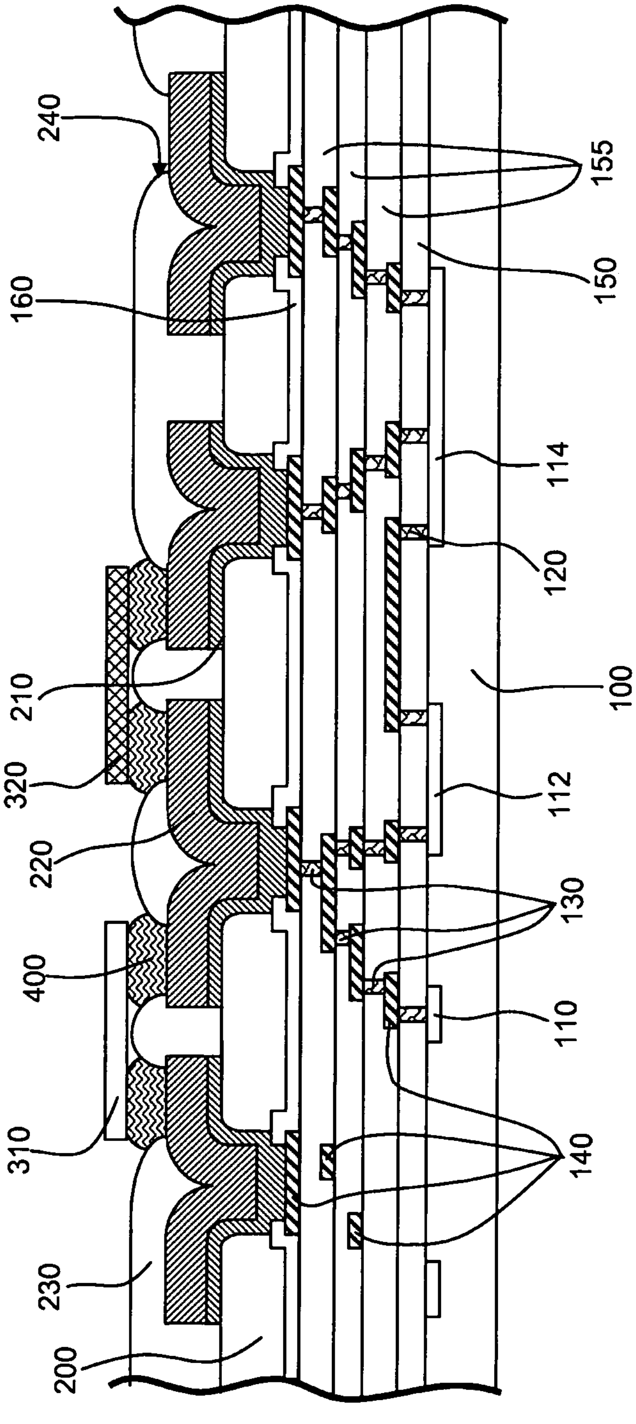
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FIG. 10

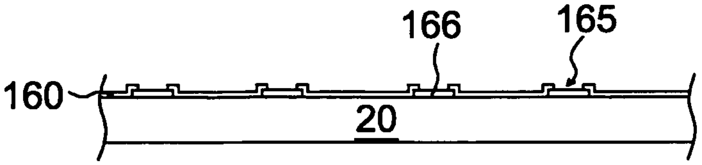

Fig. 10a

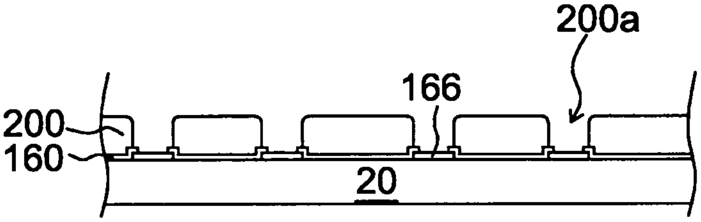

Fig. 10b

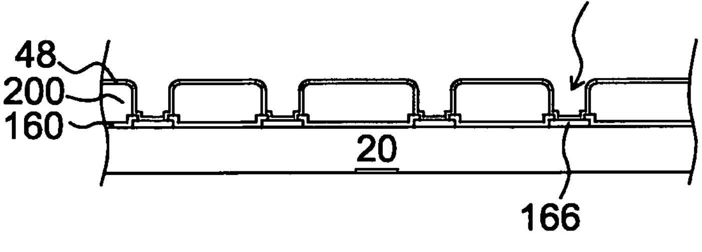

Fig. 10c

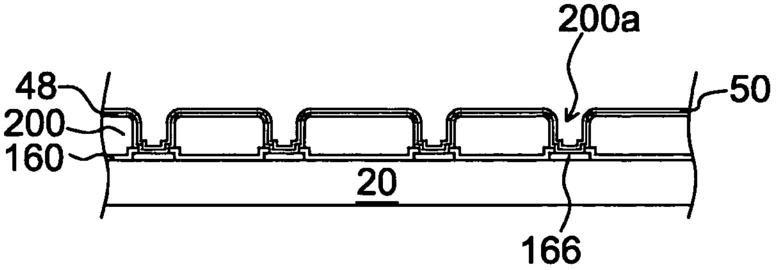

Fig. 10d

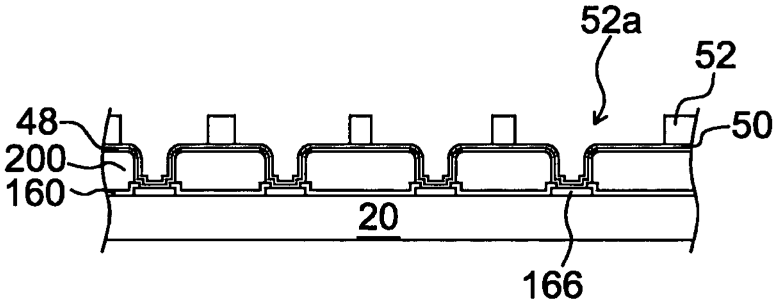

Fig. 10e

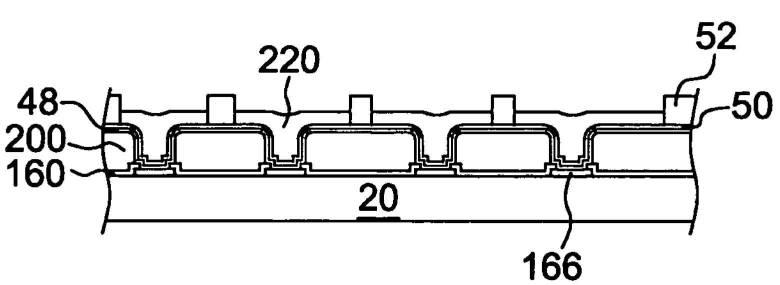

Fig. 10f

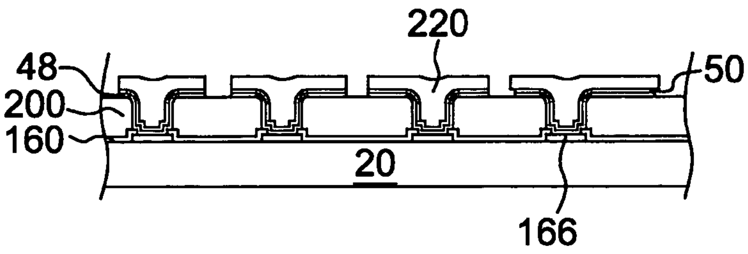

Fig. 10g

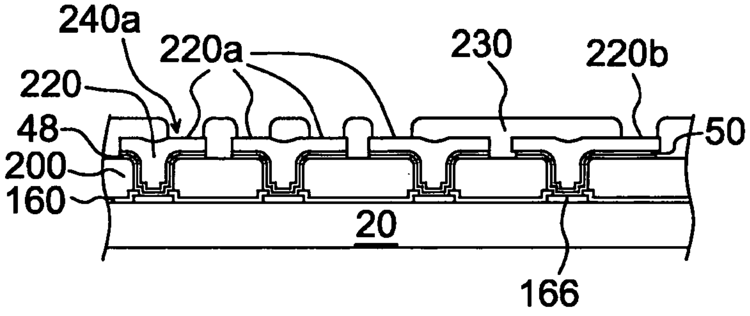

Fig. 10h

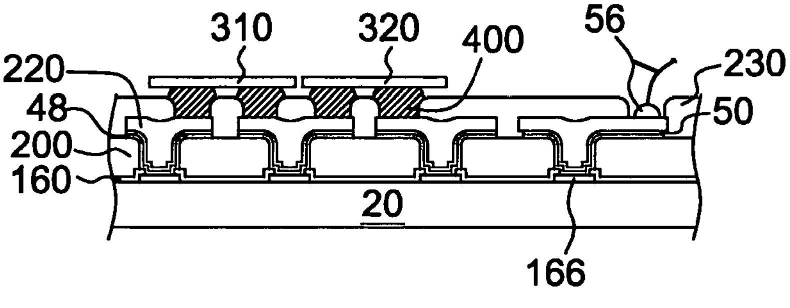

Fig. 10i

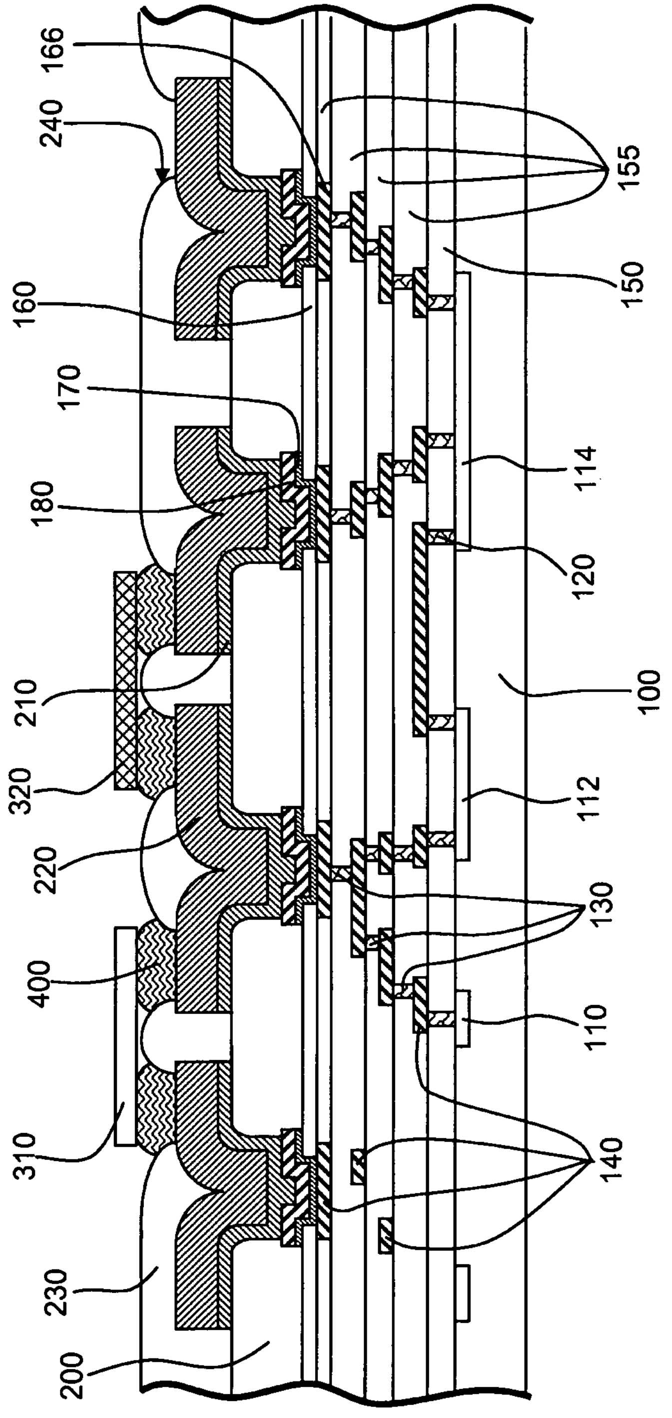
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FIG. 11a

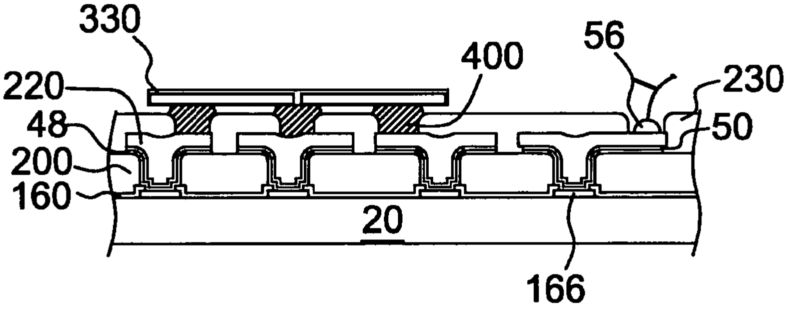

Fig. 11b

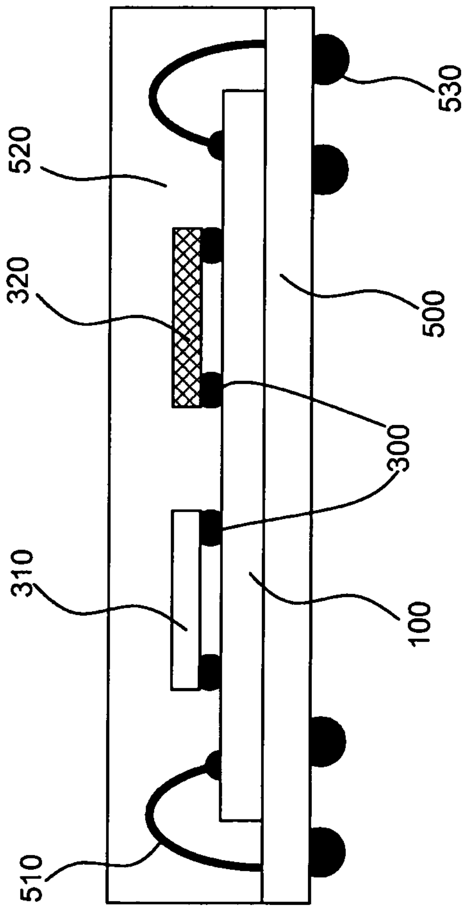

FIG. 12

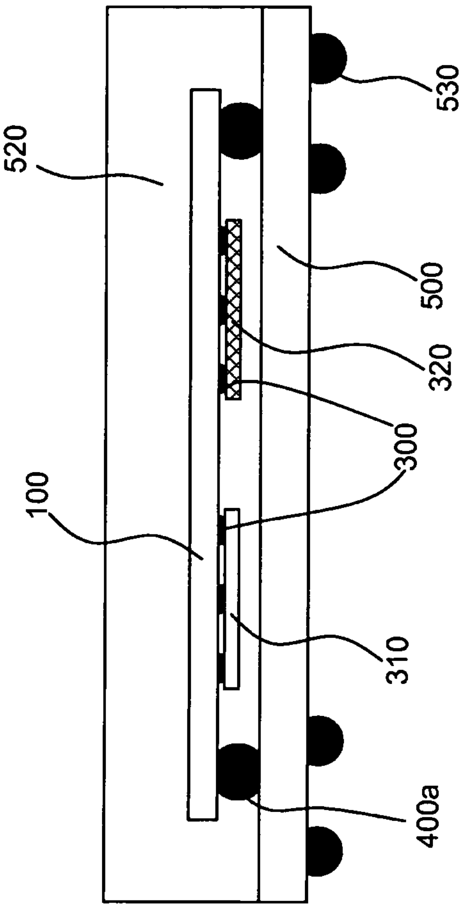

FIG. 13

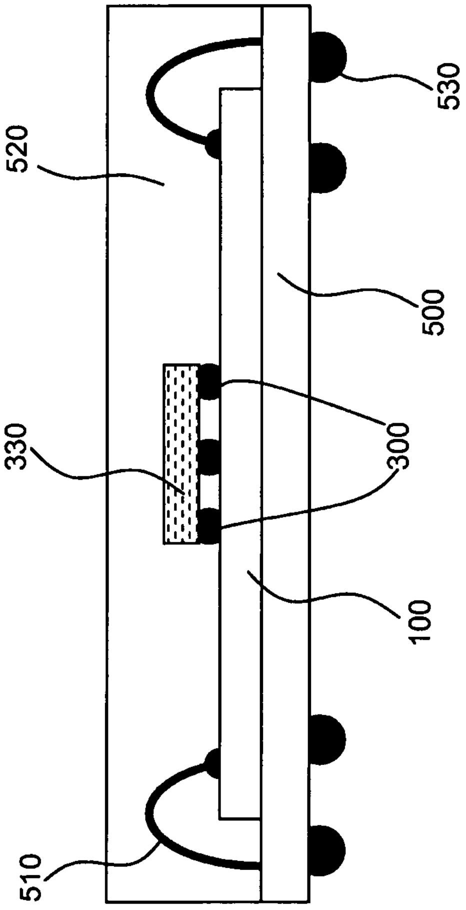

FIG. 14

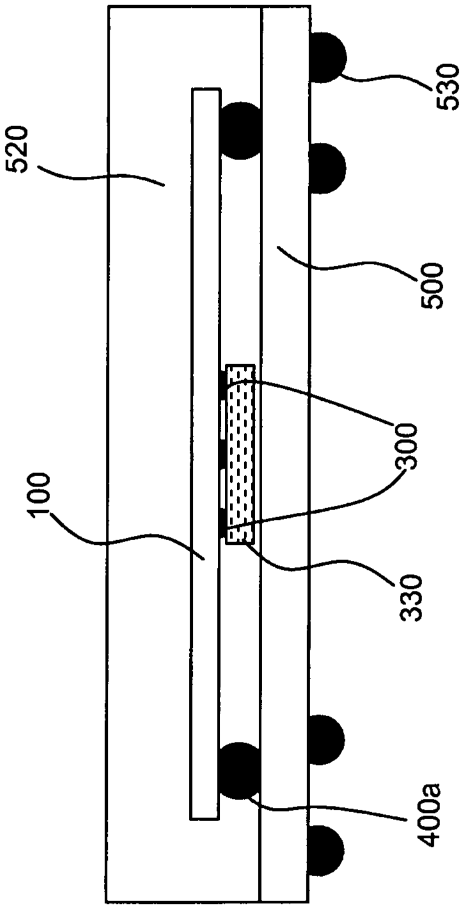

FIG. 15

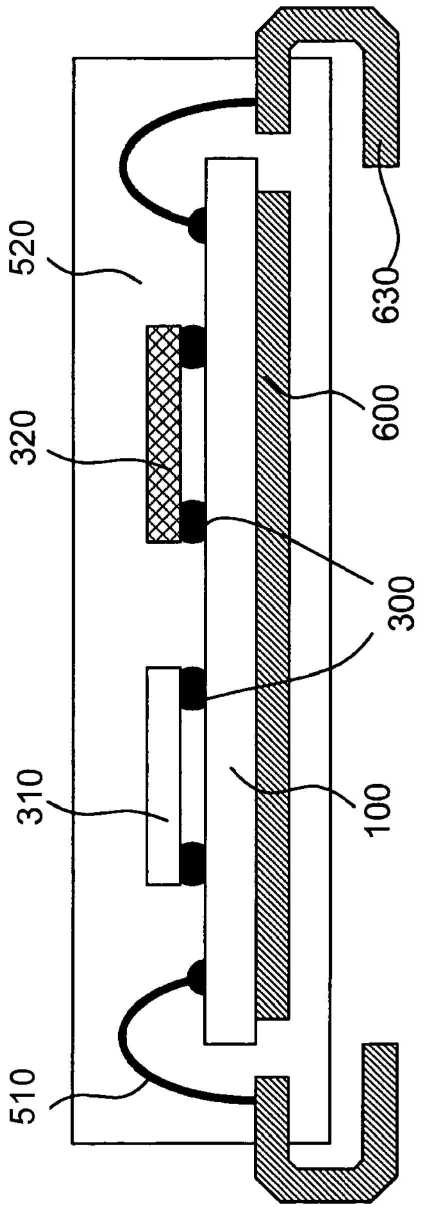

FIG. 16a

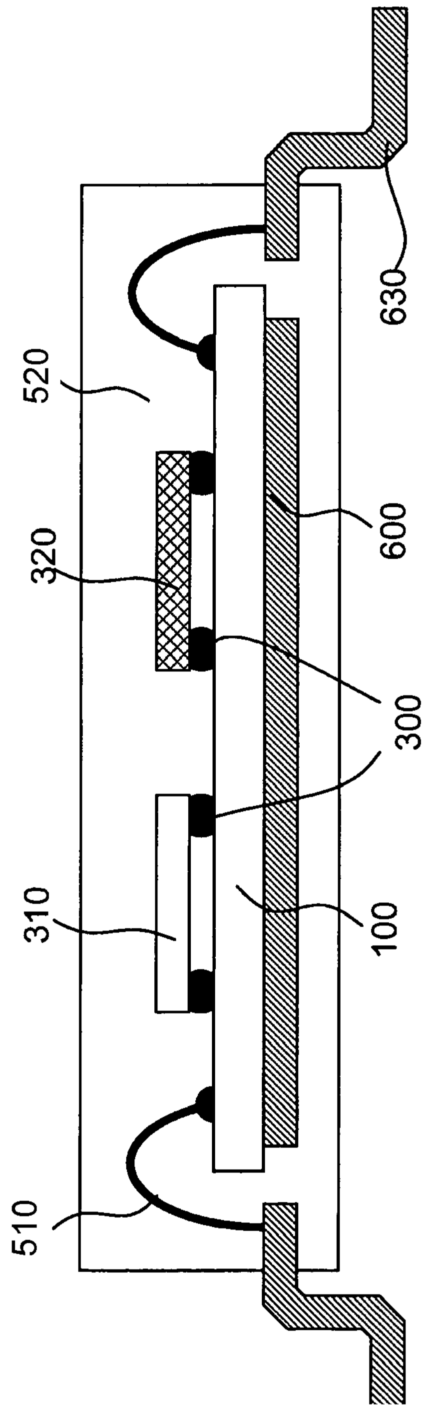

FIG. 16b

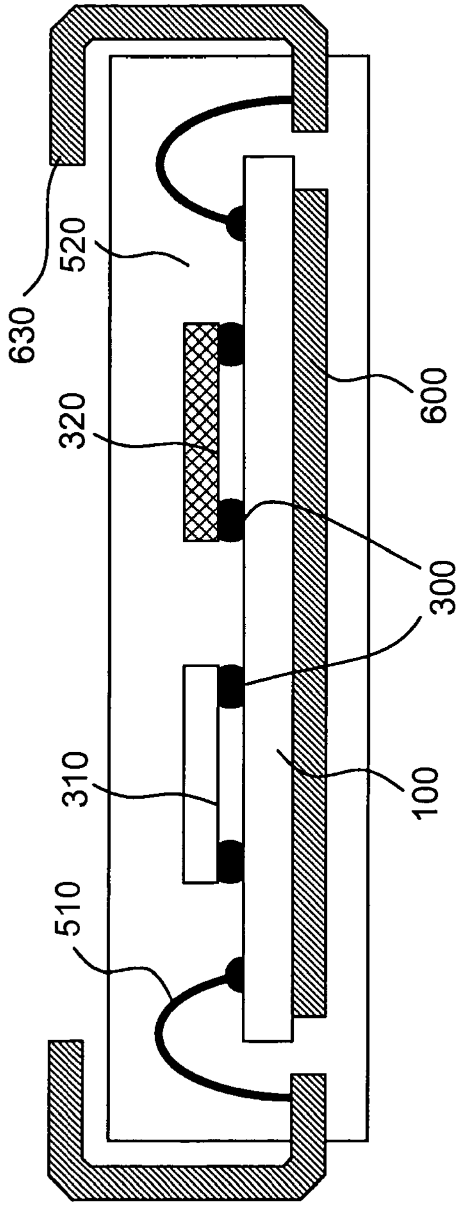

FIG. 16c

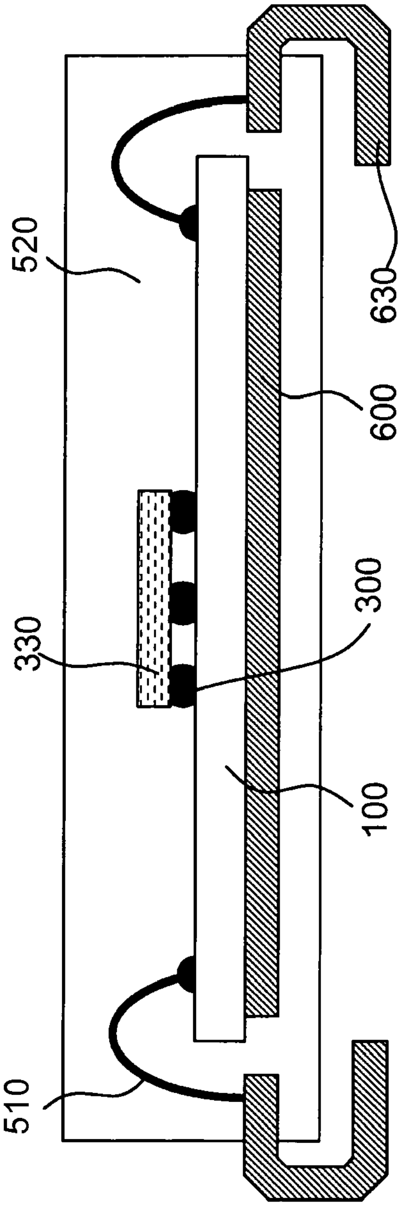

FIG. 16d

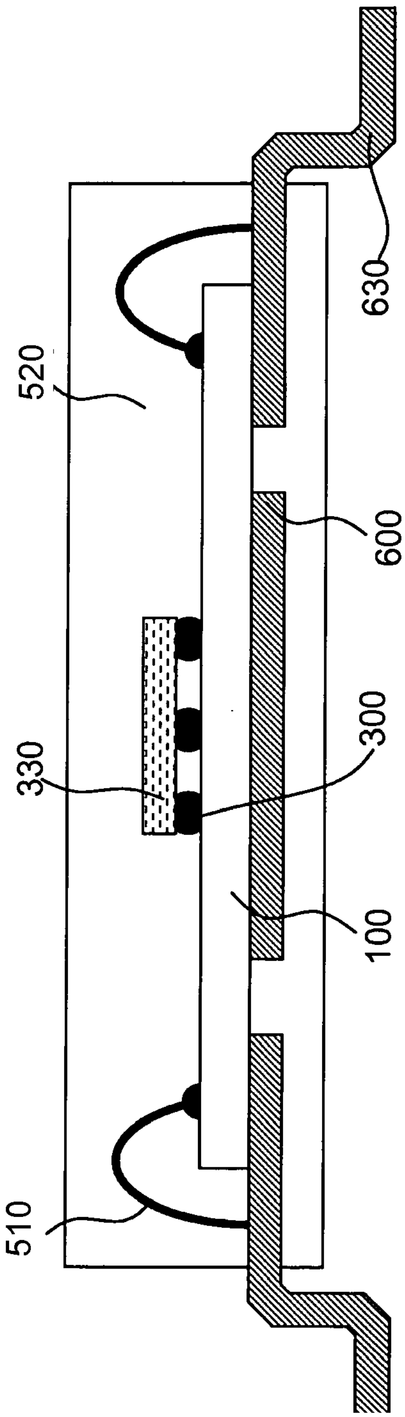

FIG. 16e

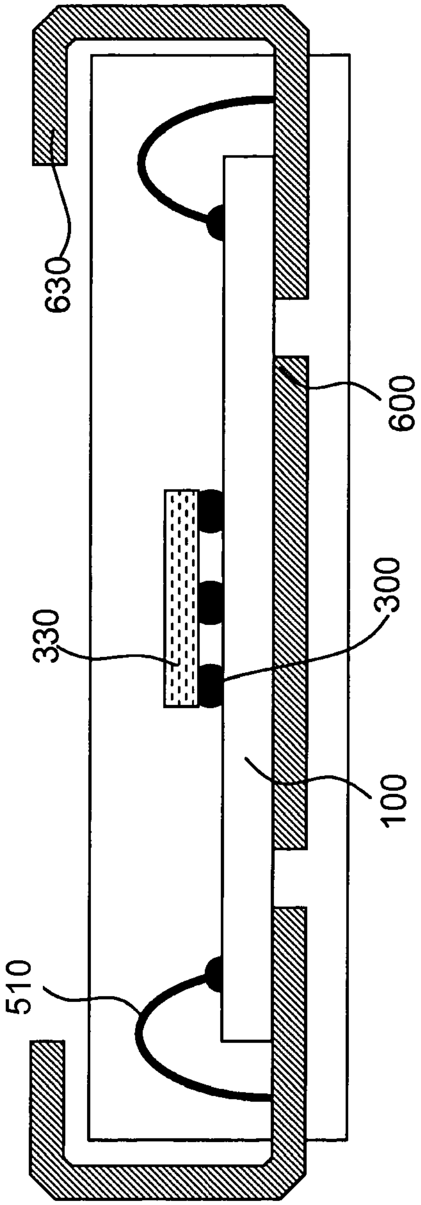

FIG. 16f

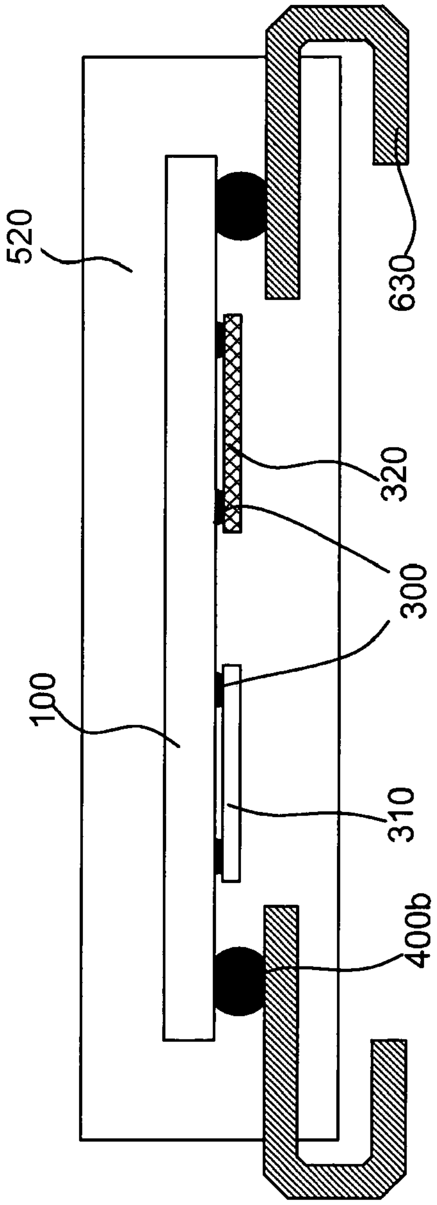

FIG. 17a

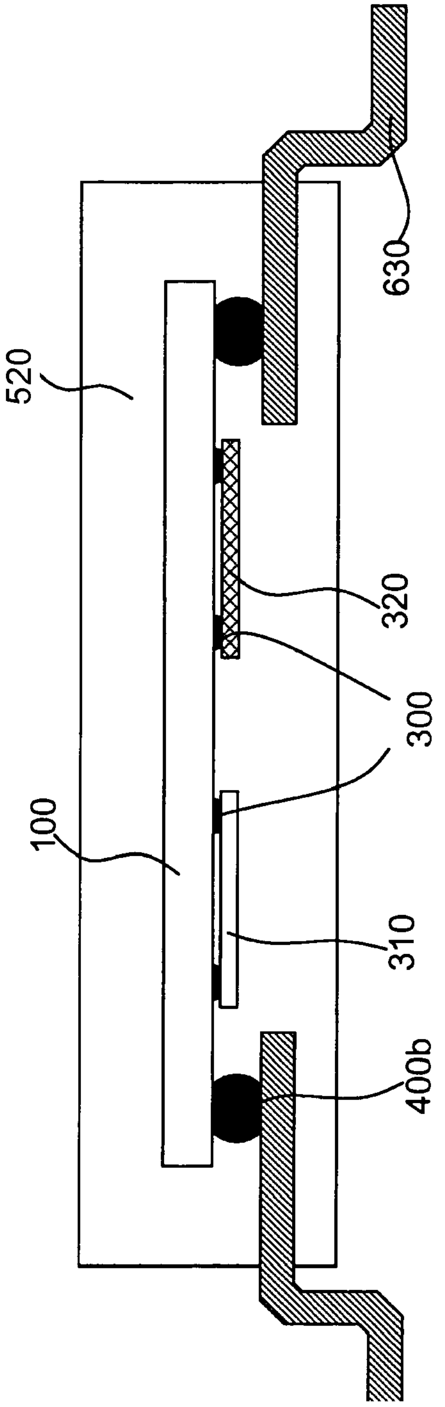

FIG. 17b

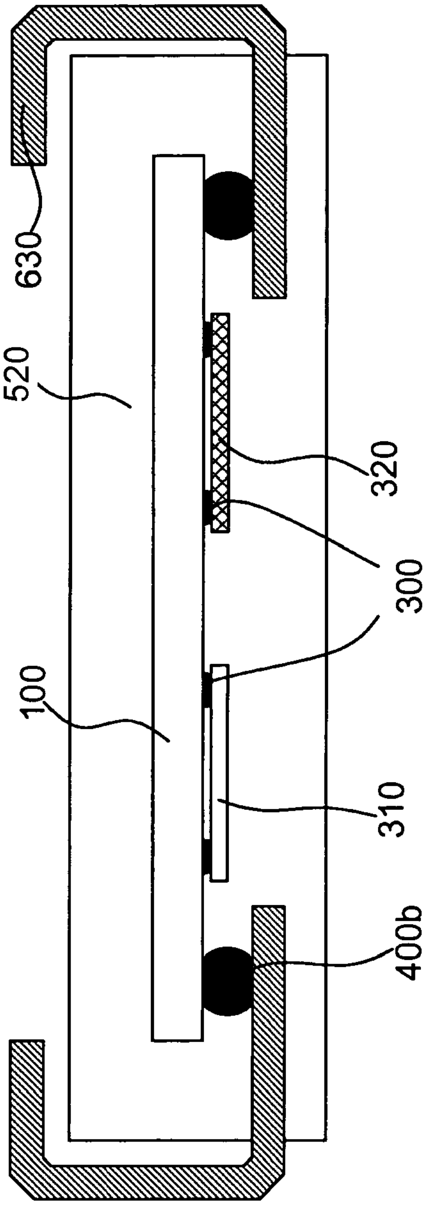

FIG. 17c

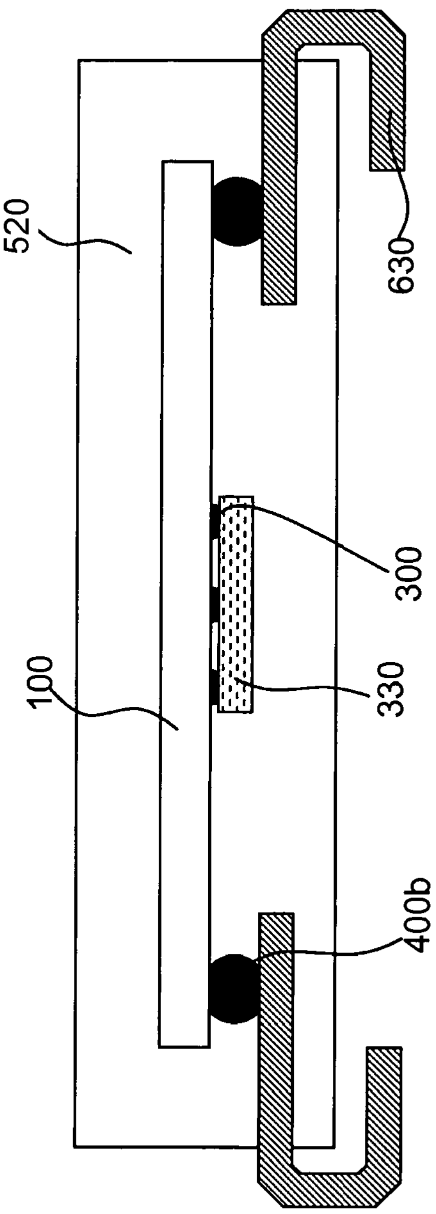

FIG. 17d

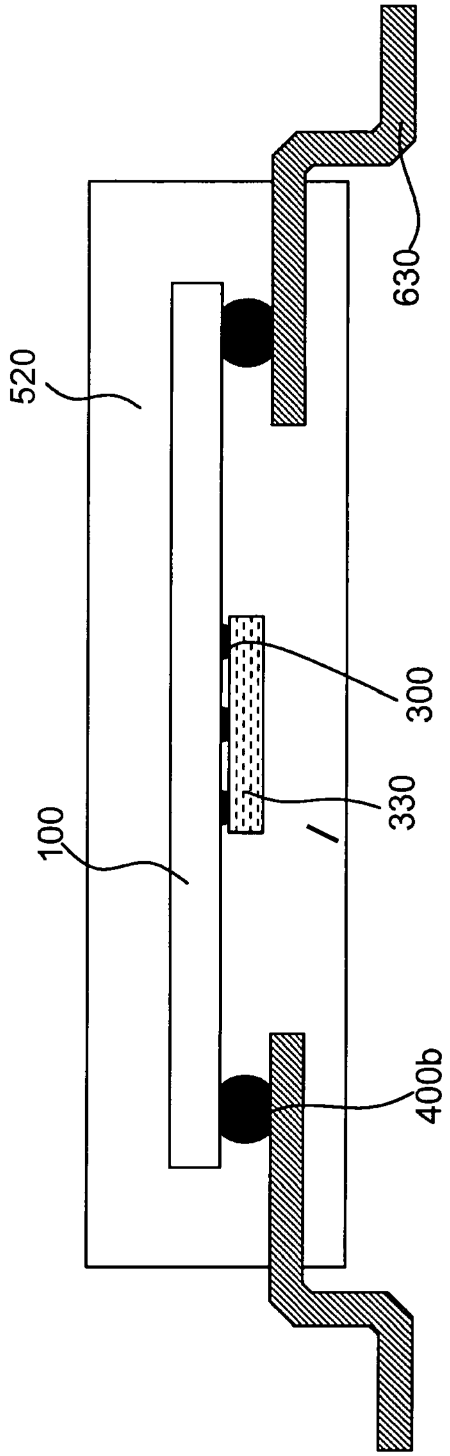

FIG. 17e

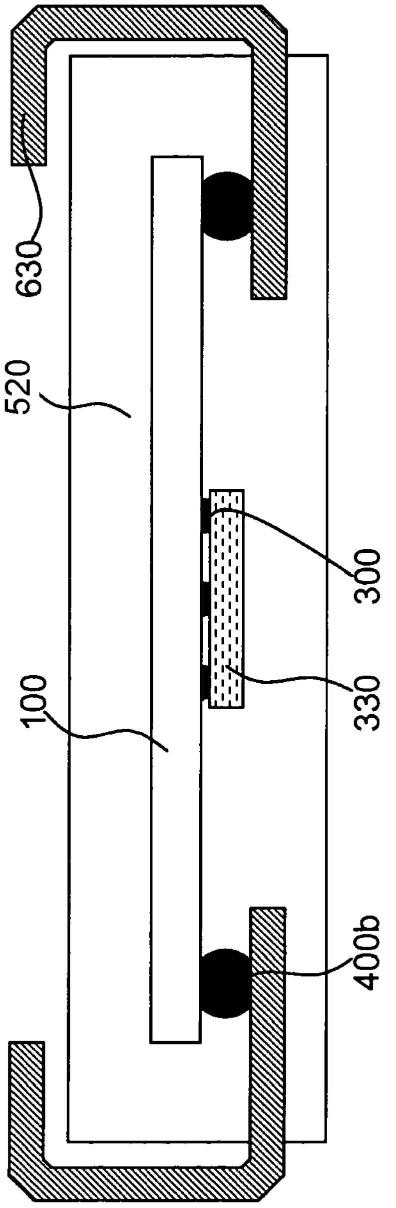

FIG. 17f

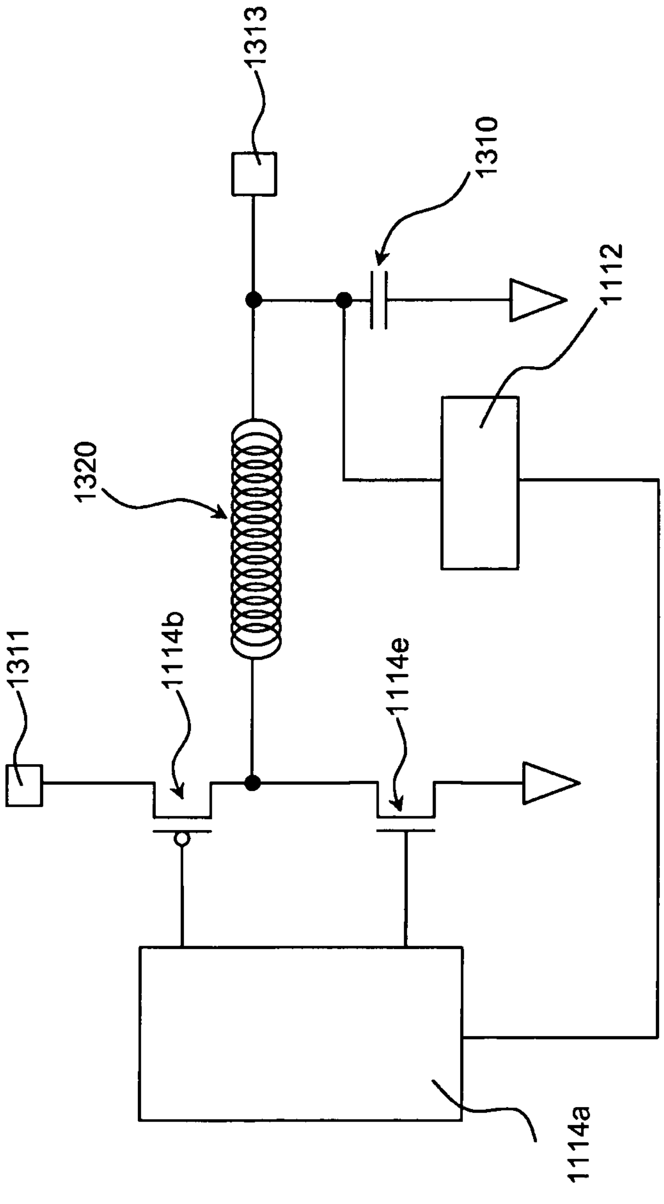

FIG. 18

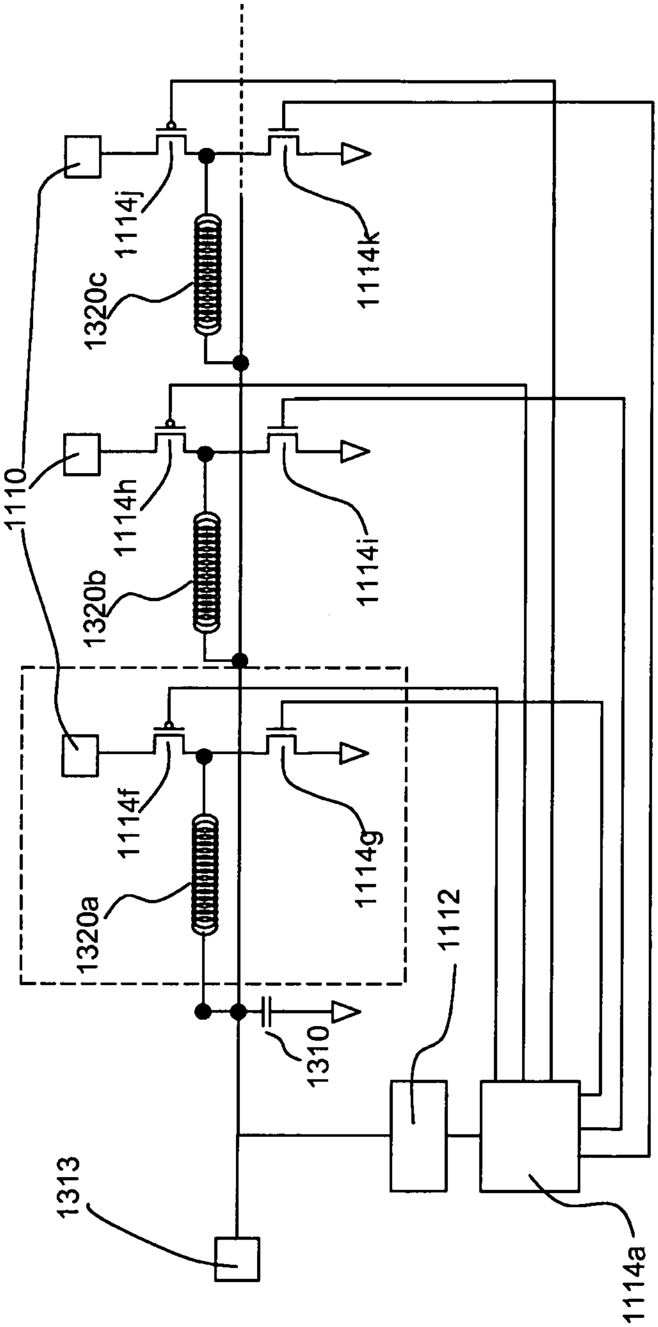
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FIG. 19

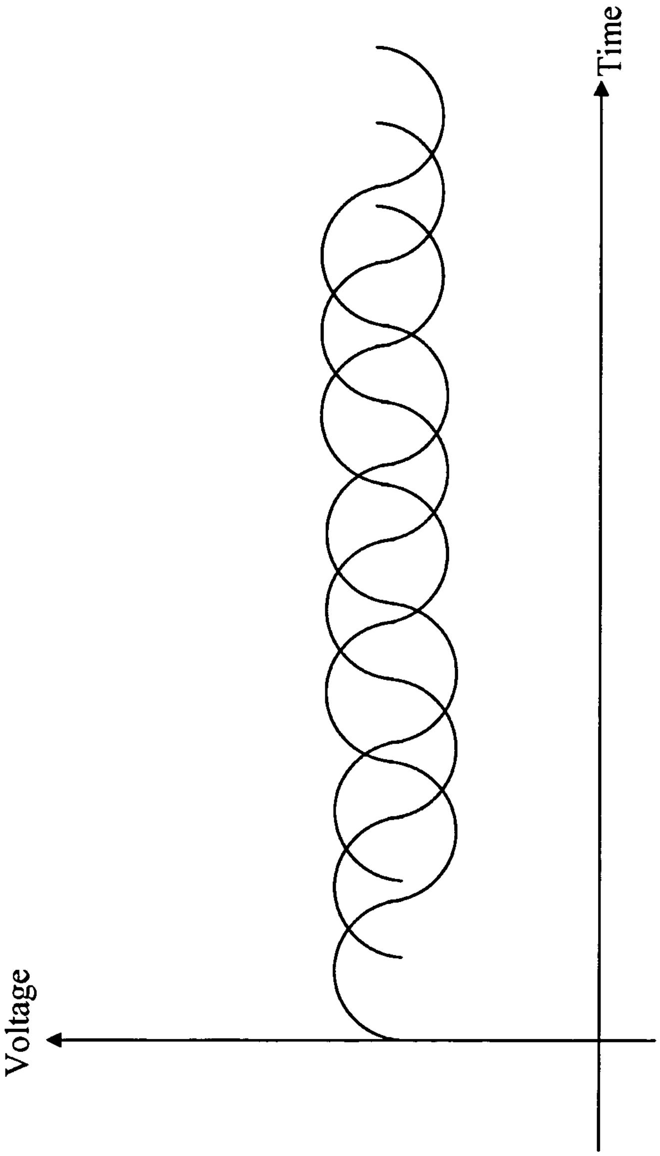

FIG. 20

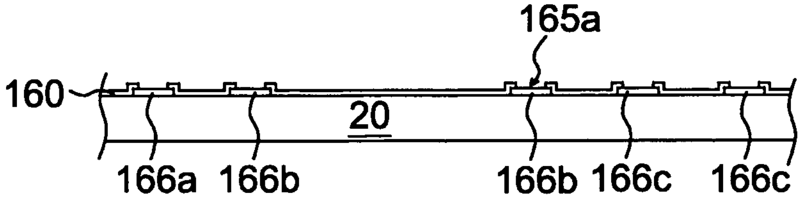

Fig.21a

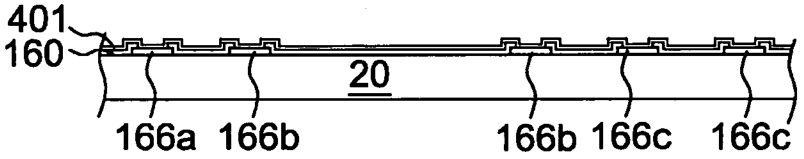

Fig.21b

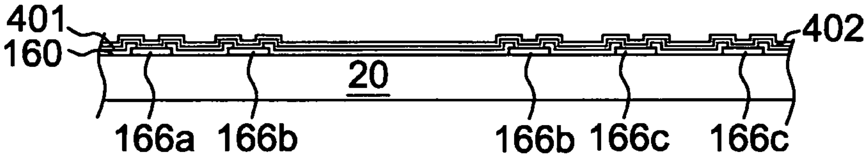

Fig.21c

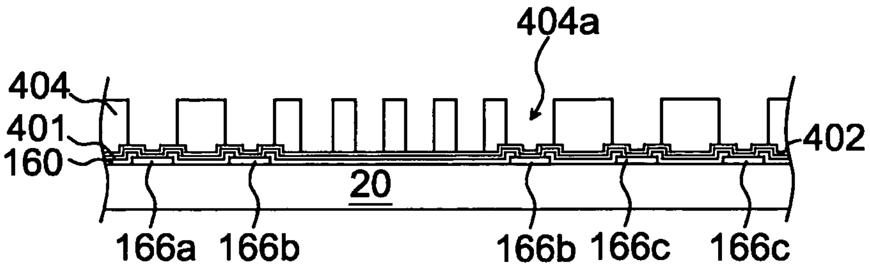

Fig.21d

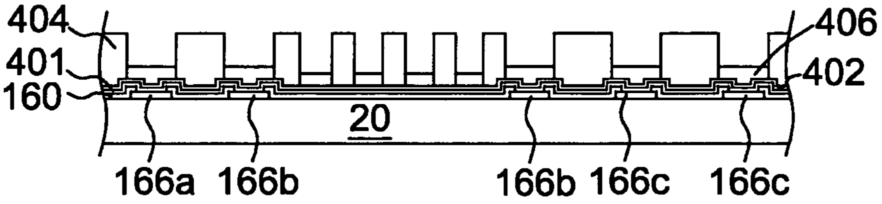

Fig.21e

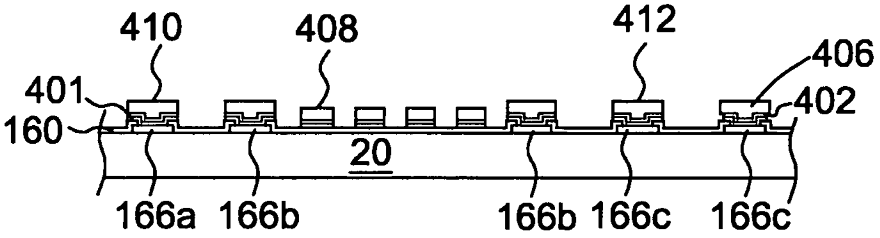

Fig.21f

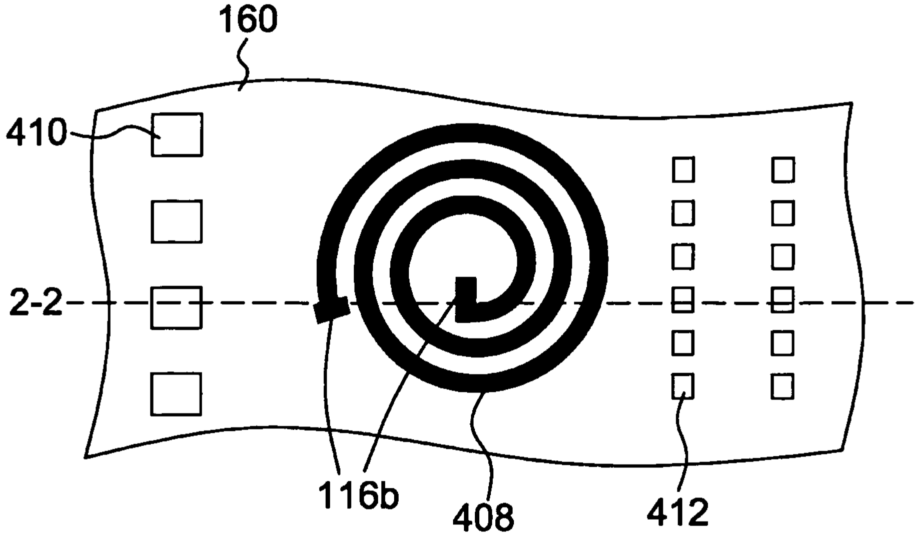

Fig.21g

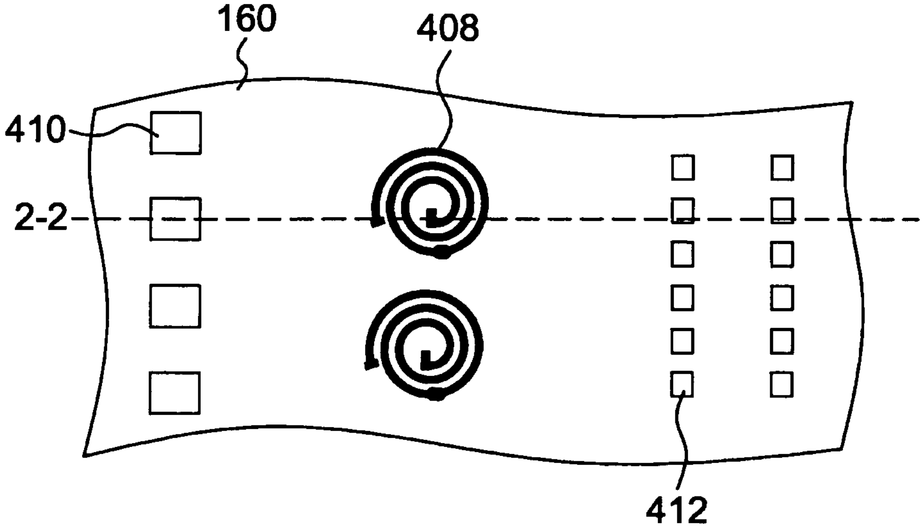

Fig.21h

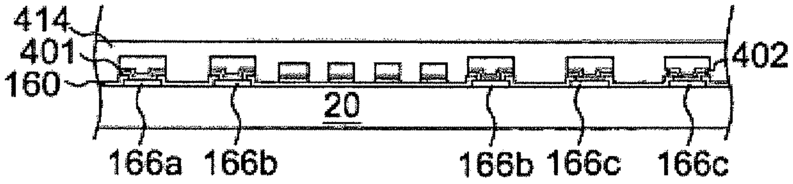

Fig.21i

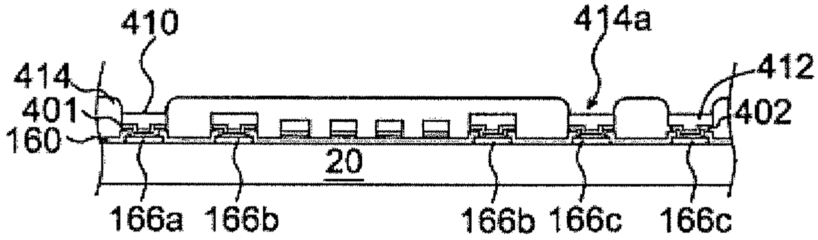

Fig.21j

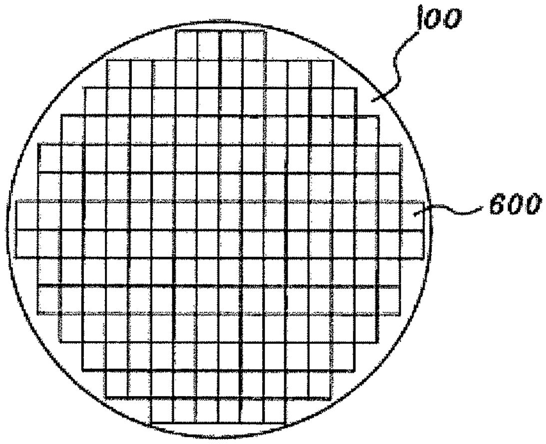

Fig.21k

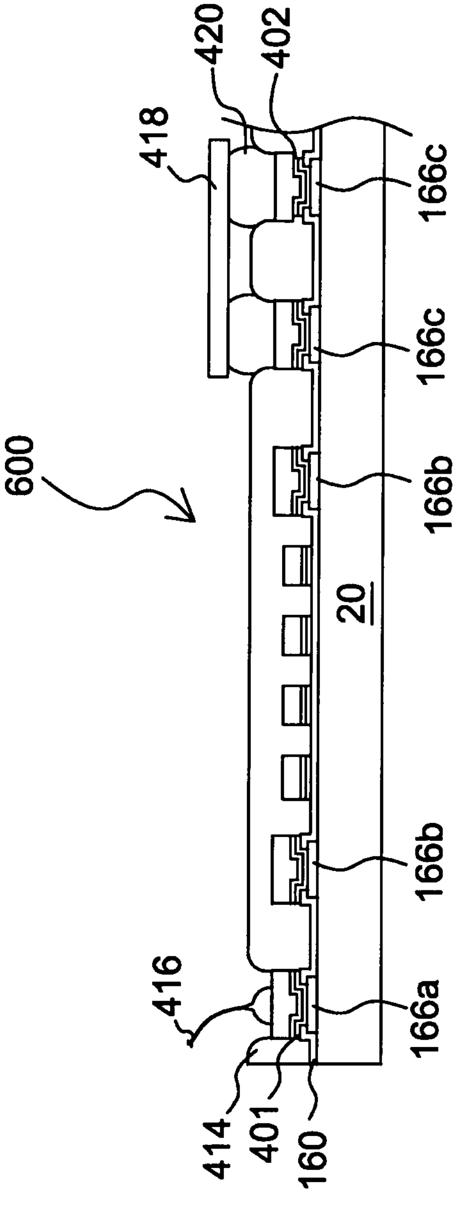

Fig.211

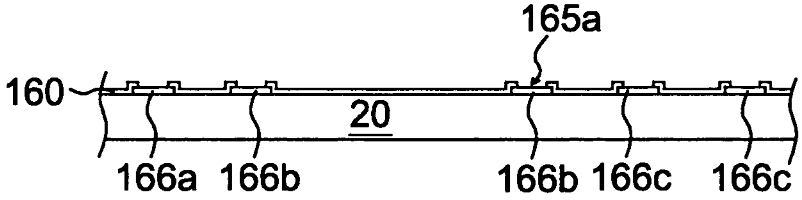

Fig.22a

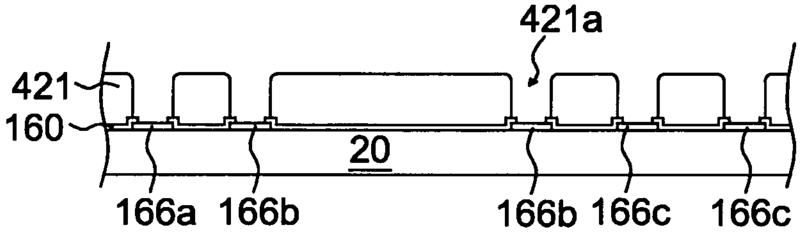

Fig.22b

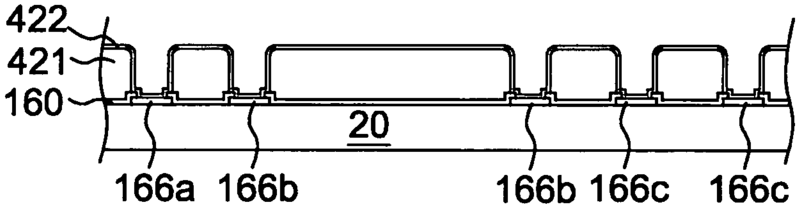

Fig.22c

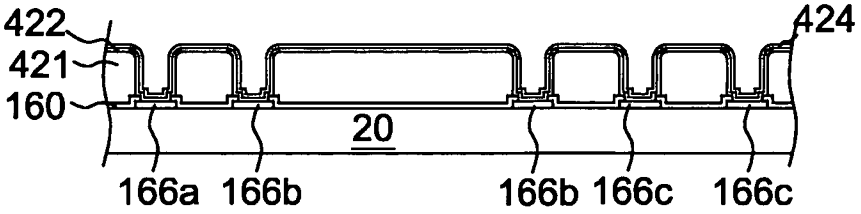

Fig.22d

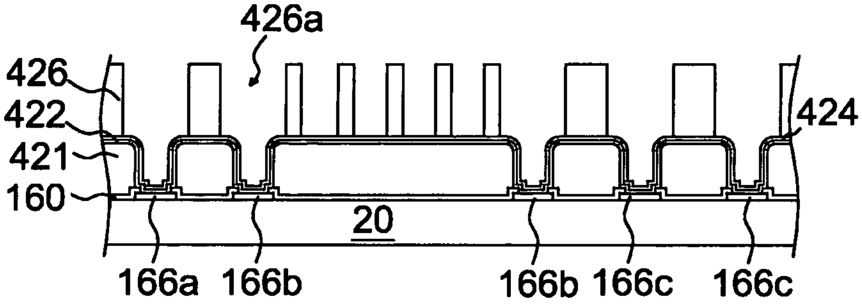

Fig.22e

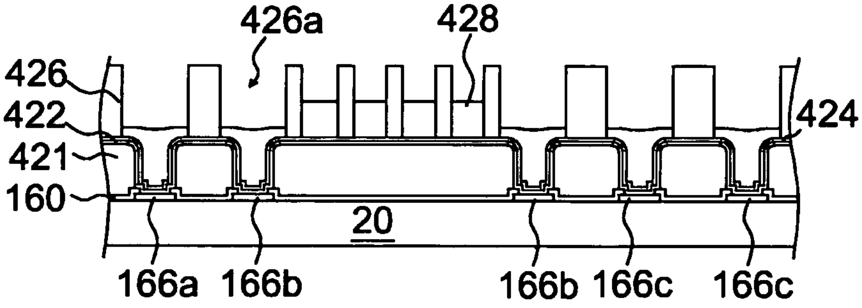

Fig.22f

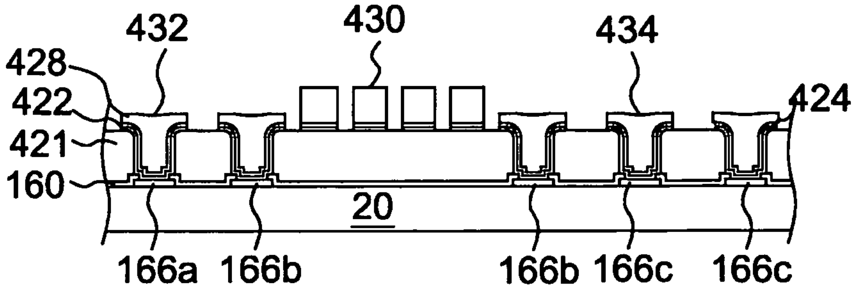

Fig.22g

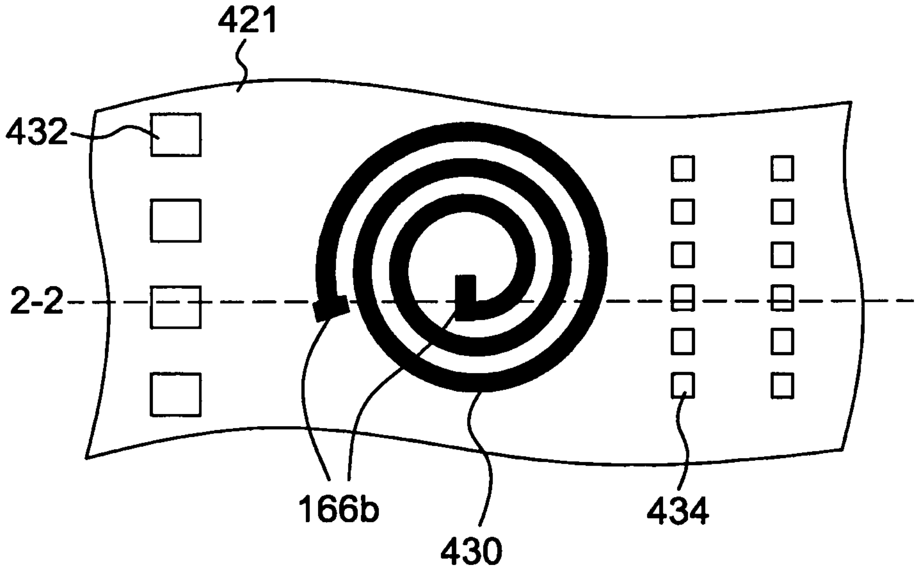

Fig.22h

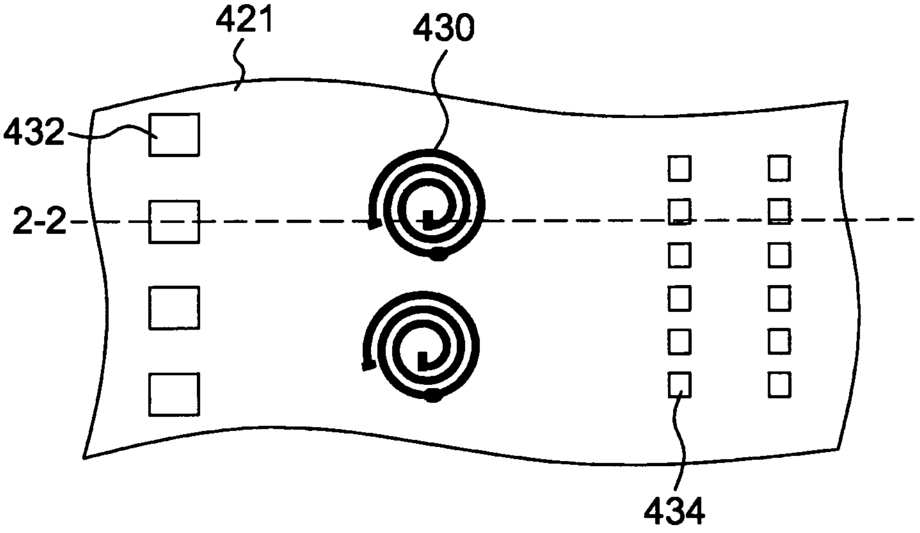

Fig.22i

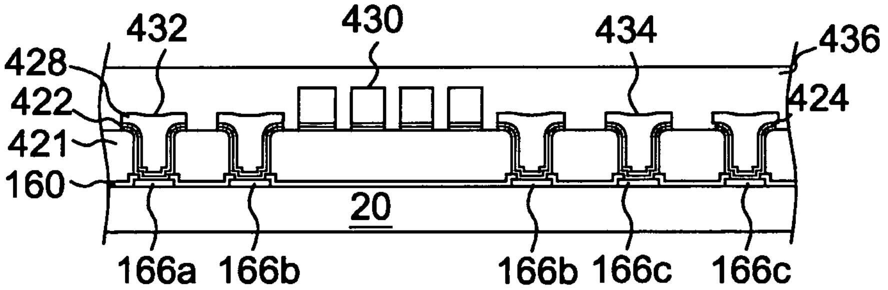

Fig.22j

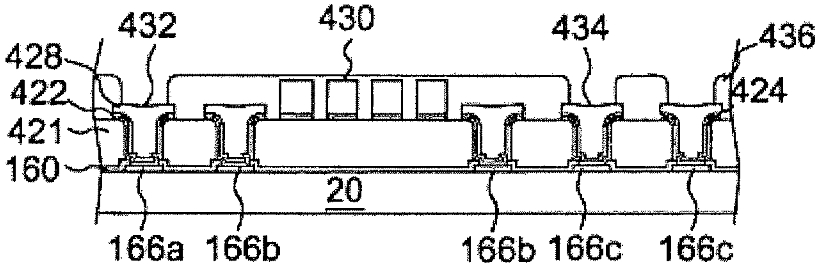

Fig.22k

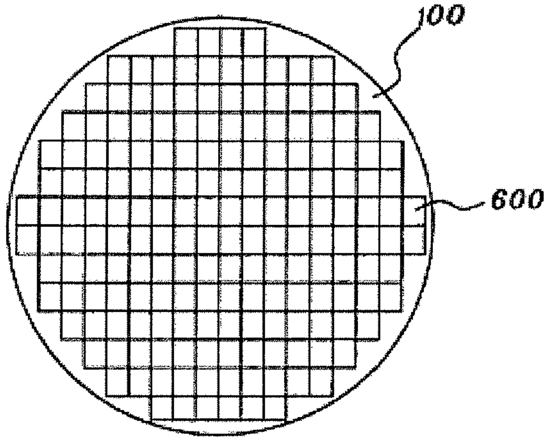

Fig.22l

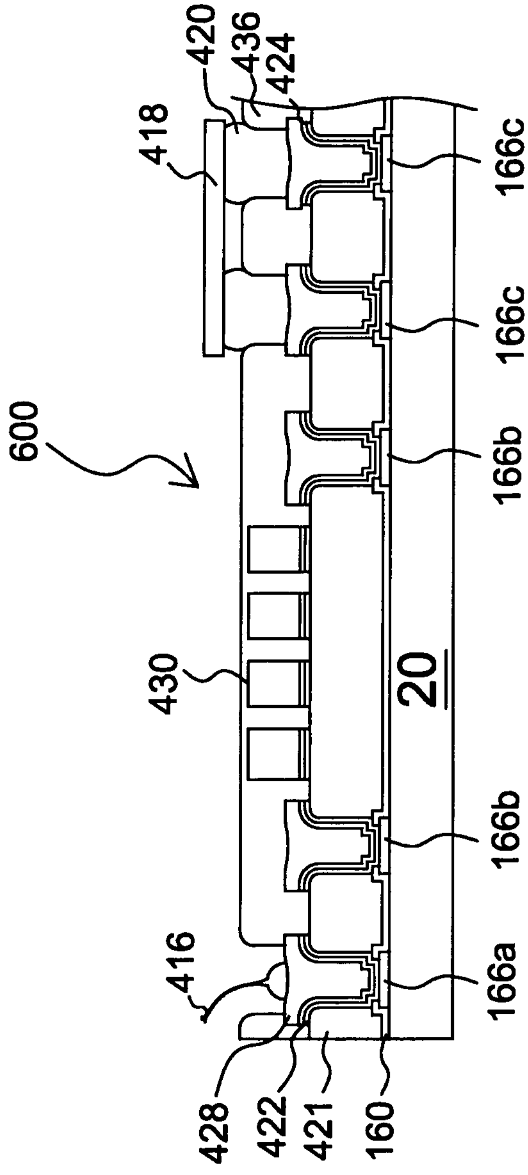
600
418
420
436
424
430
416
428
422
421
160
166a
166b
166b
166c
166c
20

Fig.22m

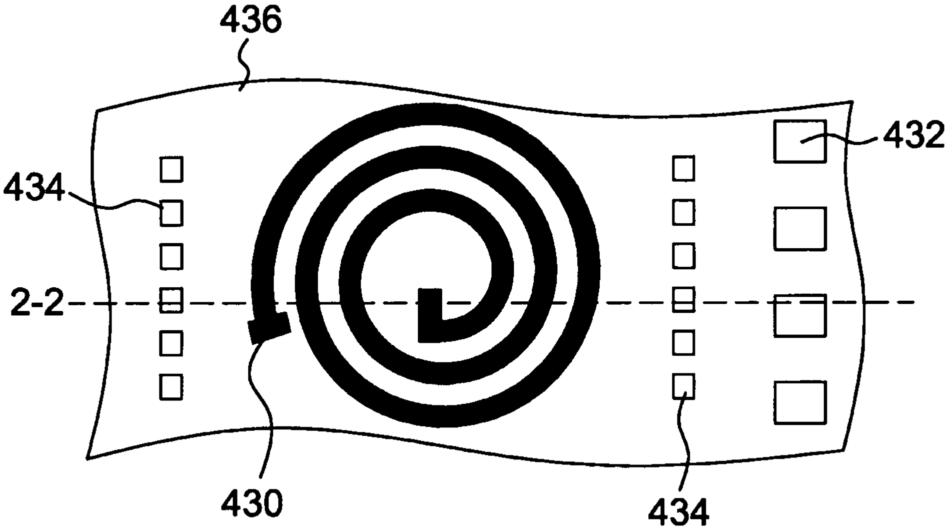

Fig.22n

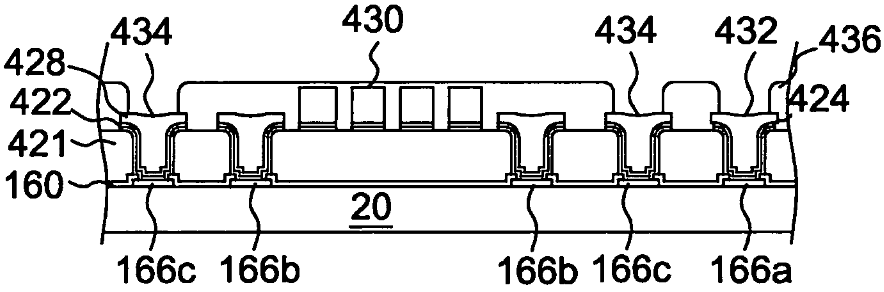

Fig.22o

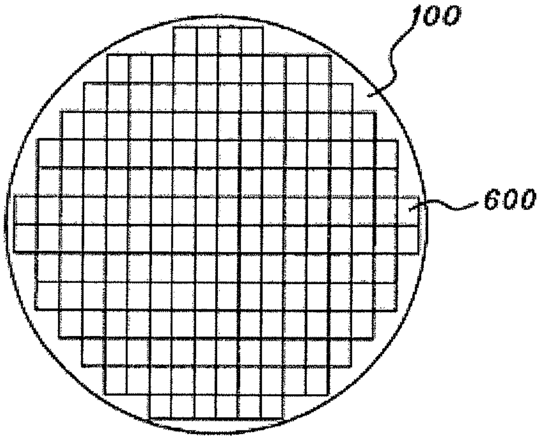

Fig.22p

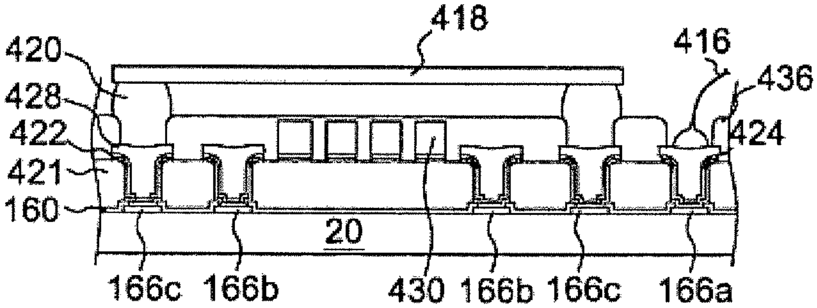

Fig.22q

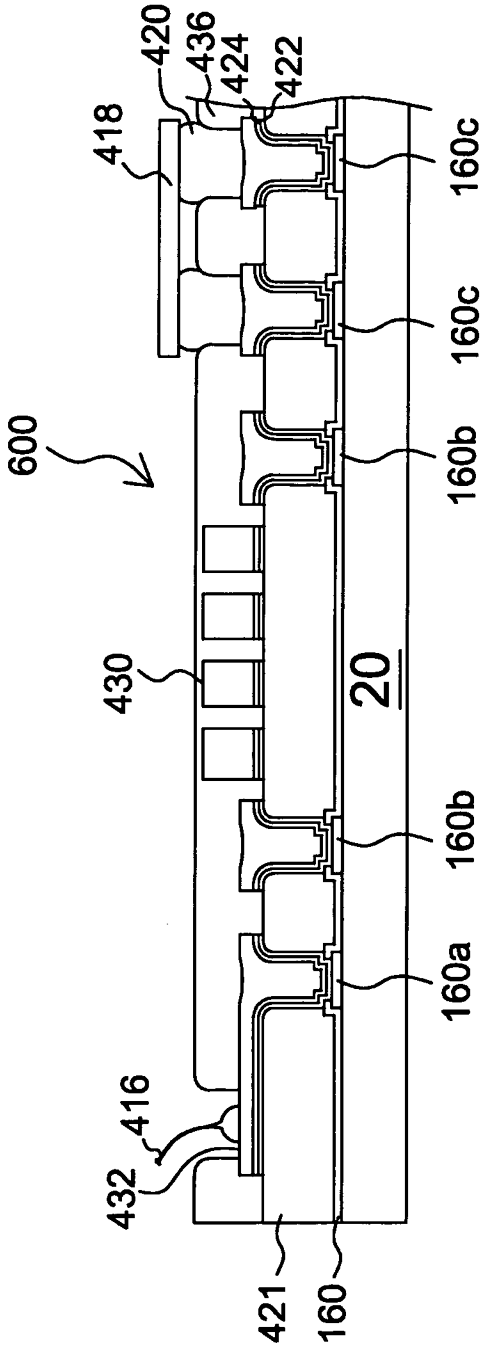
420
436
424
422
418
600
160c
160c
160b
430
20
160b
160a
416
432
421
160

Fig.23a

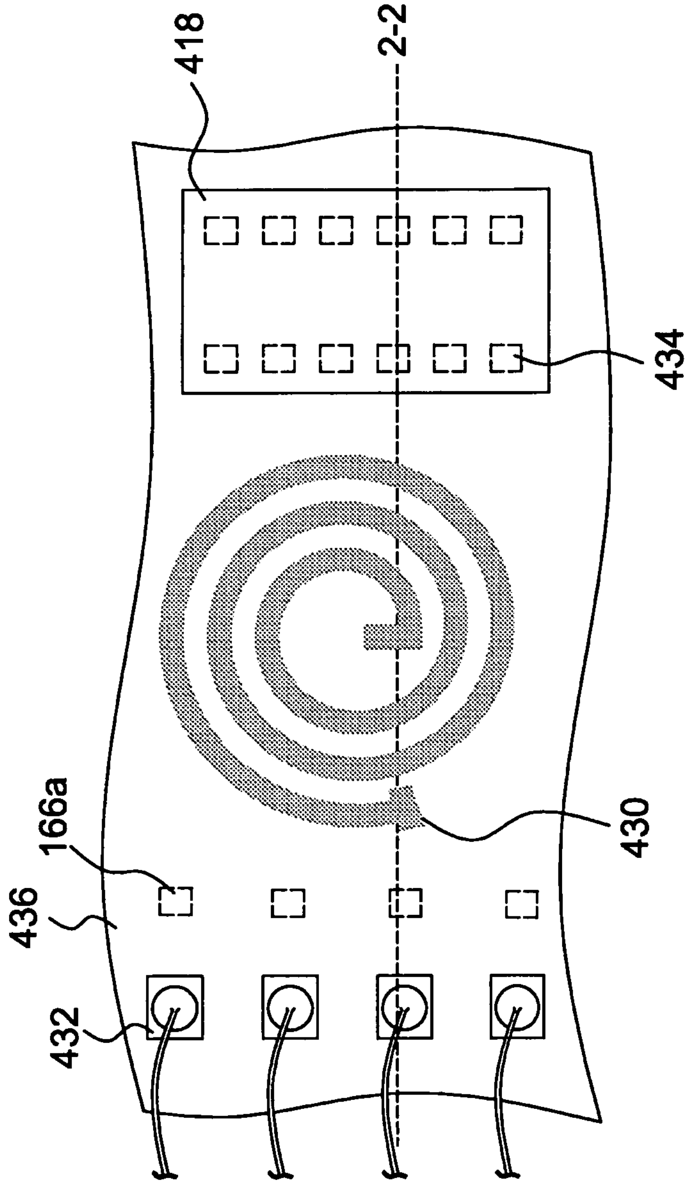

Fig.23b

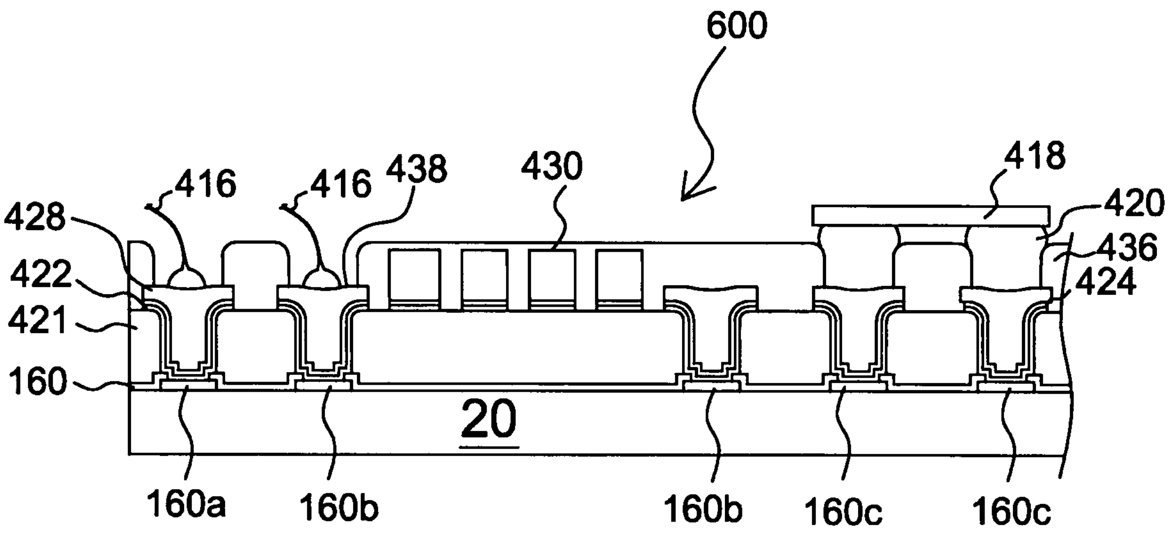
600
416
416
438
430
418
428
420
436
422
424
421
160
20
160a
160b
160b
160c
160c

Fig.24a

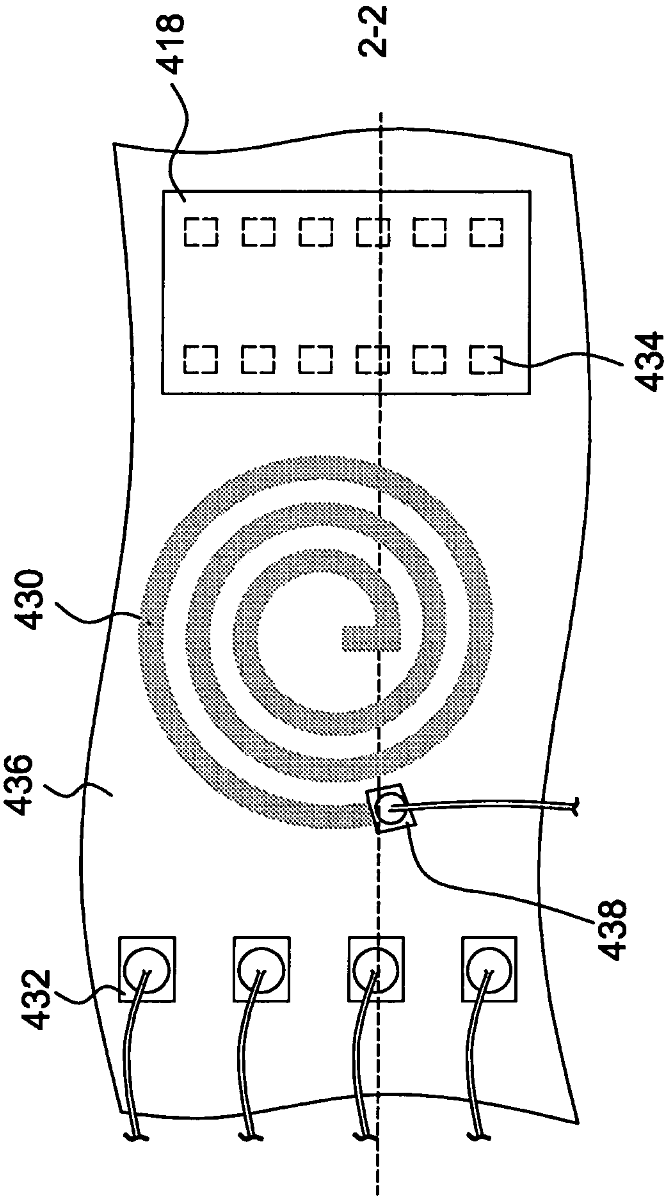

Fig.24b

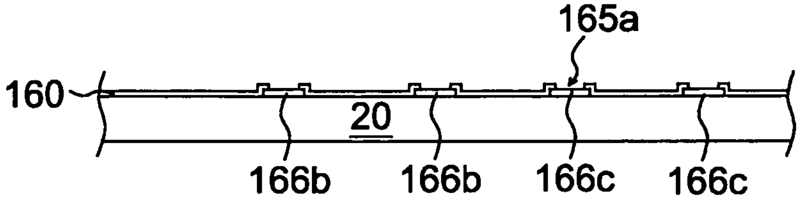

Fig.25a

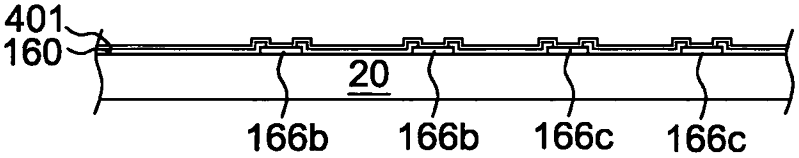

Fig.25b

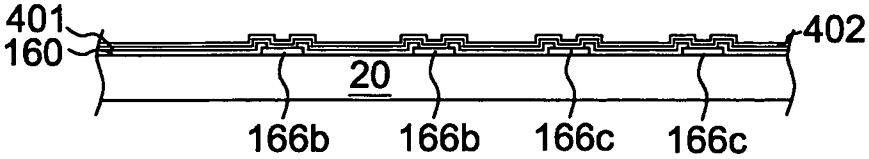

Fig.25c

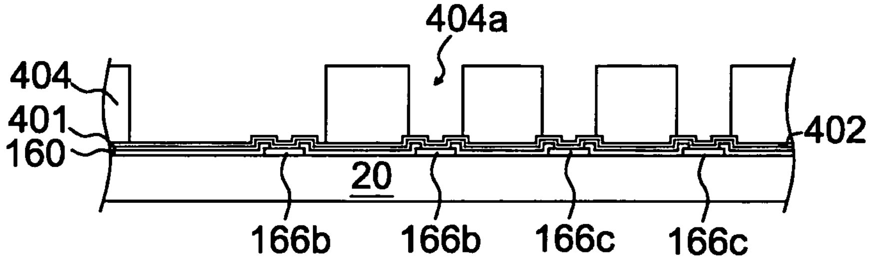

Fig.25d

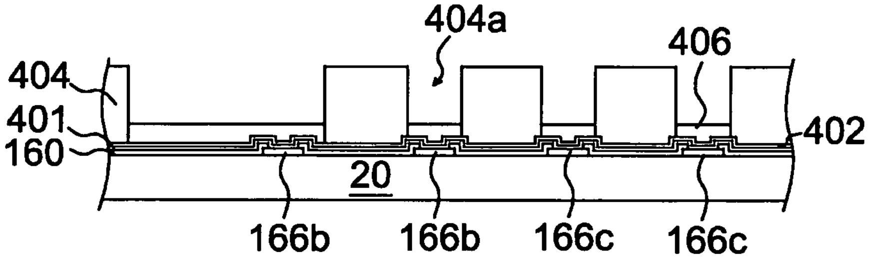

Fig.25e

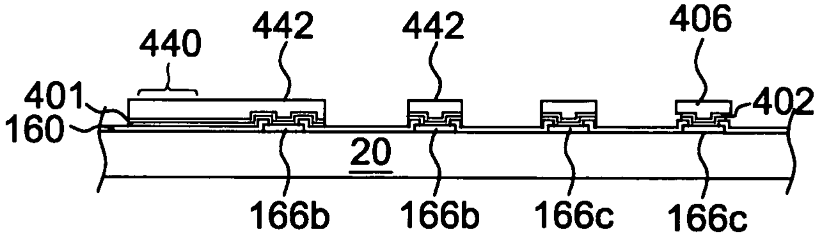

Fig.25f

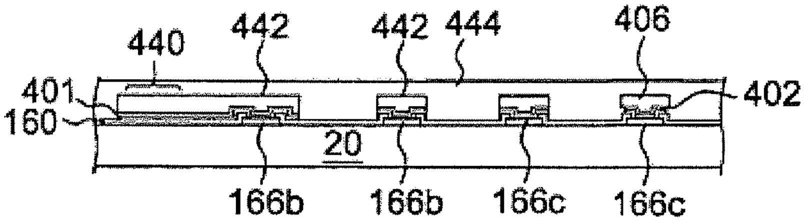

Fig.25g

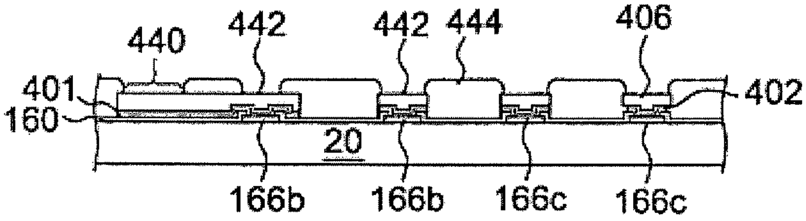

Fig.25h

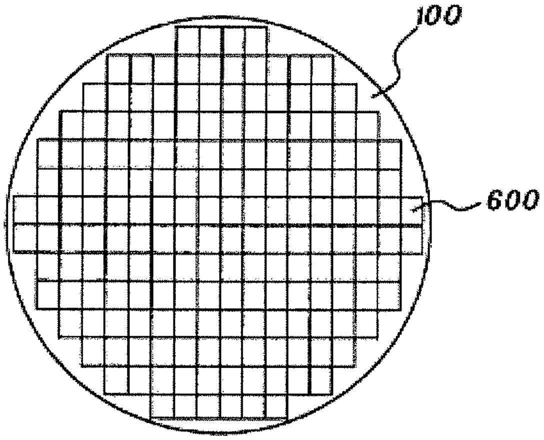

Fig.25i

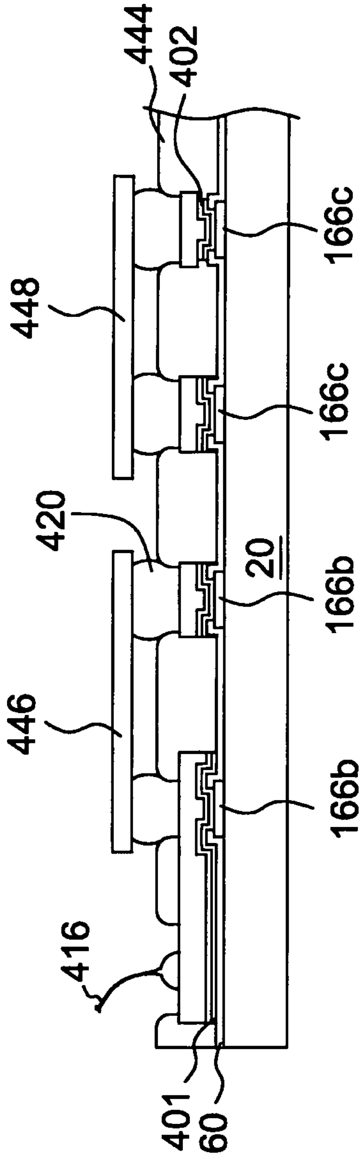

Fig.25j

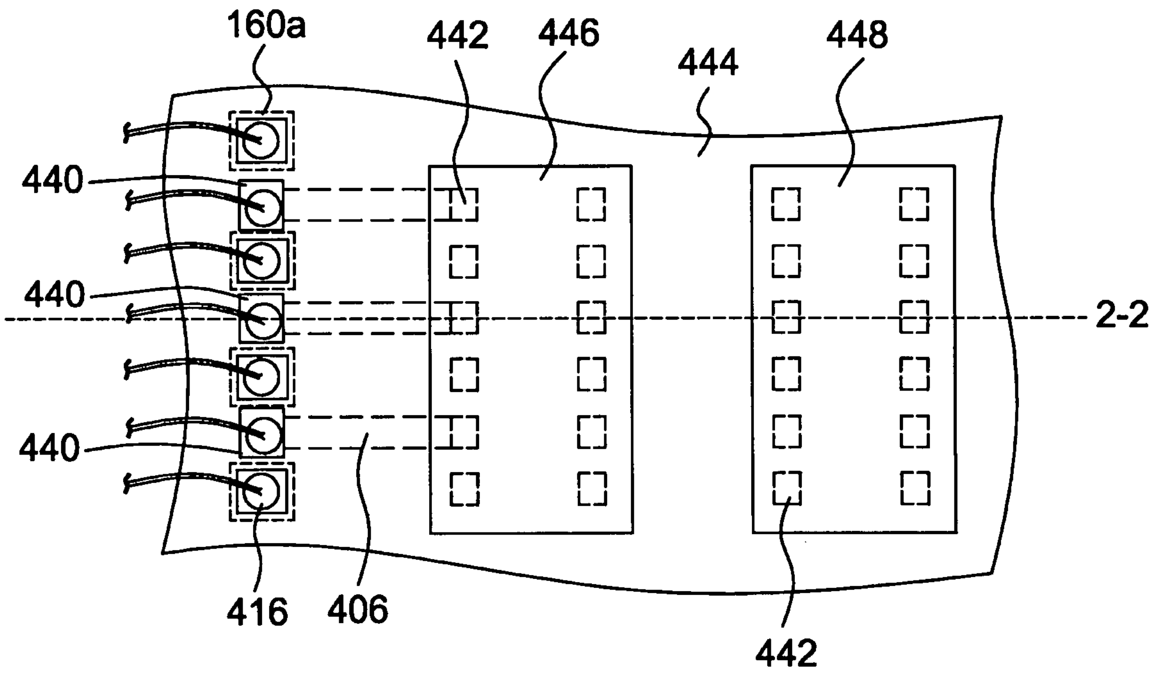

Fig.25k

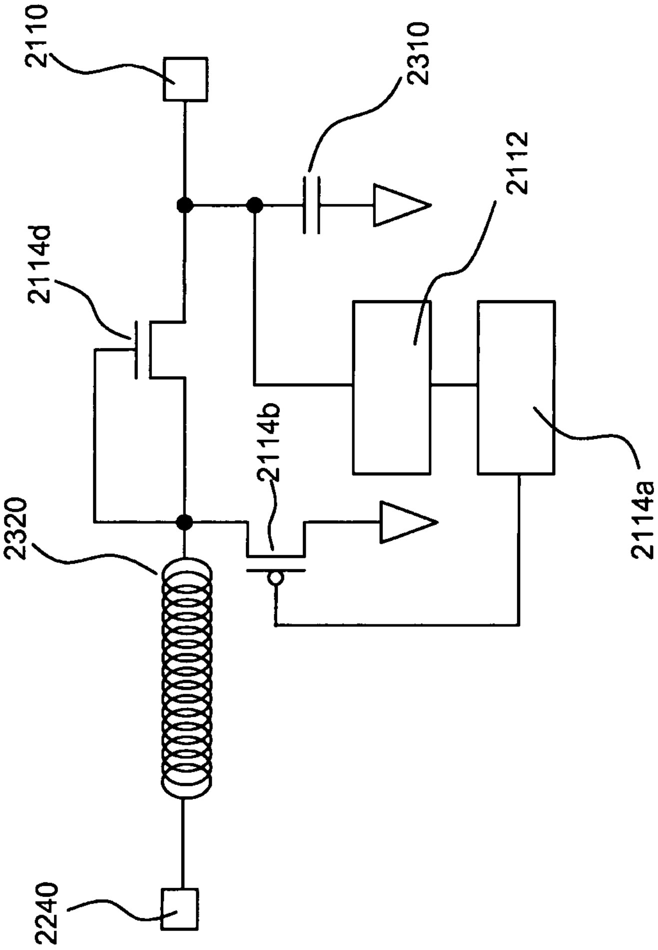

Fig. 26

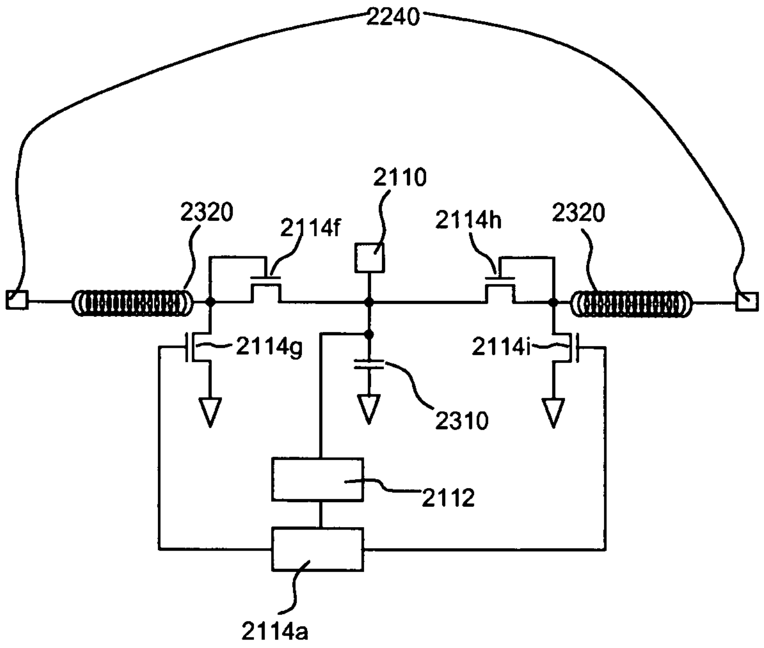

Fig. 27

VOLTAGE REGULATOR INTEGRATED WITH SEMICONDUCTOR CHIP

This application claims priority to U.S. provisional application No. 60/871,837, filed on Dec. 26, 2006, which is herein incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a type of semiconductor chip and its applications or, more specifically, it relates to a type of semiconductor chip and its application circuits.

2. Description of the Related Art

In common power regulator devices, goals behind the design not only include lowering total circuit costs, but also accelerating response speeds of signals and increasing the efficiency of regulating power supplies. Currently, in order to achieve the goal of mediating many different voltage ranges, the size of voltage regulators are rather large and on-chip regulators are not a reality. For a PCB with multiple electrical devices, because different electrical devices have different voltage demands, power supplies of different output voltages are used to correspond to general voltage ranges that are used by the electrical devices. However, this method consumes a rather large amount of energy, increases the difficulty of designing circuits, and also has a rather high cost.

Therefore, to decrease the amount of energy needed, a common method is to use multiple voltage regulators or converters to modify the voltage from a single power supply unit, in accordance to needs of the electrical devices. These voltage regulators or converters allow the voltage that enters each electrical device to correspond to the device's working voltage. For example, FIG. **1** shows a common diagram of an equivalent circuit structure. On the circuit structure, there is a power supply unit **10**, and on one side of the power supply unit **10**, a voltage regulator or converter **12** is connected. On the other side of the voltage regulator **12**, multiple parasitic elements **14** are connected, and the electrical devices **16** (such as chips) that are to be controlled are also connected to the parasitic elements. Voltage regulator **12** can vary the voltage from power supply unit **10** to a specific range that corresponds to the characteristics of electrical devices **16**.

More specifically, voltage regulator **12** can take a steady input voltage and regulate the voltage within a specific range according to the needs of different devices (such as chips), and then input the voltage into the devices. With current circuit technology, this method must be carried out by voltage regulators or converters, resistors, capacitors, and inductors constructed on the PCB. Referring to the electrical devices **16** and voltage regulator **12** disclosed in FIG. **1**, there are multiple parasitic capacitors, inductors, and resistors in serial or parallel. Therefore, after a power supply voltage is regulated by voltage regulator **12**, the power supply voltage still needs to pass through multiple parasitic elements for enabling electrical devices **16**. These multiple parasitic elements are spread out over the PCB and within the package of the chip, and therefore cause a decrease in the efficiency at which the voltage is regulated.

Referring to FIG. **2**, an example result of circuits of FIG. **1**, a graph is shown where output impedance is plotted against load current frequency. As shown on the graph, when the usage frequency of electrical devices **16** is 10^7 Hz, the corresponding output impedance is 0.025 ohms. However, when the usage frequency of electrical devices is $10^{8.5}$ Hz, the output impedance quickly increases to 0.3 ohms, showing an obvious disadvantage to this method of voltage regulation.

The circuit diagram shown in FIG. **3** is commonly used in the design of voltage regulator **12**, wherein voltage regulator **12** includes a semiconductor chip **1115**, and also an inductor **1320'** and a capacitor **1310'** constructed off-chip. Semiconductor chip **1115** includes MOS **1114*b*'**, diode **1114*c*'**, switch controller **1114*a*'**, and voltage feedback device **1112'**. Then a power supply inputs into voltage regulator **12**, voltage feedback device **1112'** takes a voltage signal and transfers it to switch controller **1114*a*'**. Switch controller **1114*a*'** then uses this voltage signal to control when MOS **1114*b*'** is switched on or off, which therefore controls the output voltage.

Another circuit diagram is shown in FIG. **4**. This circuit diagram is similar to that of FIG. **3**, except that the diode **1114*c*'** in FIG. **3** is replaced by MOS **1114*d*'** in FIG. **4**. In this circuit, the voltage feedback device **1112'** also takes a voltage signal and transfers it to switch controller **1114*a*'**, which controls when MOS **1114*b*'** is switched on or off, therefore controlling the output voltage.

Therefore, the greater the number of different types of electrical devices **16** on the PCB, the greater the number of corresponding voltage regulating devices, so that the supply voltages entering the electrical devices **16** will fall in the correct voltage range. However, such circuit design utilizes a large quantity of high cost voltage regulator devices, and the electrical wiring between different voltage regulators **12** must be separated, causing the need for more metal lines and therefore increasing total manufacturing costs. Needless to say, such circuit design is not suitable for use in micro-scale electronic products. In addition, although the use of multiple voltage regulators **12** in place of multiple power supply units **10** can effectively reduce the amount of resources wasted, the large number of voltage regulators **12** used to account for different electrical devices **16** causes circuits on the PCB to become rather complicated. Because signals pass through a complicated arrangement of wiring, the signal response time is naturally longer and cannot be immediate, simultaneously lowering efficiency of power management. Also, the circuit design takes up a large portion of the PCB, which is an inefficient use of circuit routing.

The present invention proposes a semiconductor chip and its application circuit to lessen above mentioned problems.

SUMMARY OF THE INVENTION

The primary objective of the present invention is to provide a semiconductor chip structure and its application circuit, wherein the switching voltage regulator or voltage converter is integrated within the semiconductor chip using chip fabrication methods, so that the switching voltage regulator or voltage converter and semiconductor chip are combined as one structure.

Another objective is to provide a semiconductor chip structure and its application circuit, with the ability to adapt immediately to supply-voltage variation, efficiently decreasing the transient response time.

Still another objective is to provide a semiconductor chip structure and its application circuit, so that the use of such semiconductor chip with the integrated voltage regulator or converter will reduce the overall difficulty of circuit designs on the PCB or Motherboard, both satisfying the demand to lower manufacturing costs and miniaturize electronic products.

In order to achieve the above mentioned objectives, the present invention provides a semiconductor chip structure, which includes a silicon substrate with multiple devices, and a set of external components. On this silicon substrate there is a thin circuit structure with a passivation layer. This passivation layer has multiple passivation layer openings for electrically connection from external components or circuits to the thin circuit structure. The above mentioned devices are active devices. Examples of active devices include diodes, P-Type MOS devices, N-type MOS devices and complementary metal oxide semiconductor (CMOS) devices. Voltage feedback devices and switch controller are composed of the mentioned active devices in the semiconductor chip. On the other hand, external components are passive components, such as the resistors, capacitors, and inductors. From bottom to top, the circuit structure includes at least the first dielectric layer, first metal layer, second dielectric layer, and second metal layer. The first dielectric layer lies above the substrate, and within the first dielectric layer there is a contact window. The first metal layer is above the first dielectric layer, and every point on the first metal layer can be electrically connected to corresponding devices using corresponding contact windows. The second dielectric layer is above the first metal layer and contains multiple vias [Do we need to define via?]. The second metal layer is above the second dielectric layer, and every point on the second metal layer can be electrically connected to corresponding first metal layer through corresponding vias. Also, on the passivation layer there is a polymer layer. This polymer layer has an opening above the opening of the passivation layer, and an under bump metal structure or post passivation metal layer is constructed on top of the passivation layer opening. Also, according to different semiconductor chips, there are a solder layer, or a solder wetting layer, or a wire bondable layer, a barrier layer, a metal layer and an adhesion/barrier layer comprised in the under bump metal structure. The thickness of the solder layer can vary depending on the different thicknesses of and materials used in the packaging structure of semiconductor chips. The post passivation metal layer may has the same composition as the under bump metal structure or comprises with an adhesion/barrier layer and a metal layer that is a copper or gold. Lastly, on the post passivation metal layer there is a second polymer layer, and this second polymer layer contains an opening that allows the post passivation metal layer to be revealed. Also, the semiconductor chip in the present invention uses methods used in the Thin Small Outline Package (TSOP), Small Outline J-Lead (SOJ), Quad Flat Package (QFP), Think Quad Flat Package (TQFP), or Ball Grid Array (BGA) as packaging methods. In addition, using wire-bonding or flip chip techniques, the semiconductor chip in the present invention is electrically connected to the outside.

The present invention also provides the application circuit of a semiconductor chip, which includes an internal electrical circuit and an external electrical circuit. The internal and external circuits are electrically connected using a metal circuit. The devices of the internal circuit are chosen from, but not limited to, P-Type MOS devices, N-type MOS devices, CMOS devices, voltage feedback devices and switch controller. On the other hand, components of the external electrical circuit are chosen from, but not limited to, resistors, capacitors and inductors. The internal electrical circuit is in or over a silicon substrate, while the metal circuit and external circuit are over said substrate with the metal circuit in between the internal circuit and external circuit. Similarly, all semiconductor chips in the present invention use methods used in the Thin Small Outline Package (TSOP), Small Outline J-Lead (SOJ), Quad Flat Package (QFP), Think Quad Flat Package (TQFP), or Ball Grid Array (BGA) as packaging methods. In addition, using wire-bonding or flip chip techniques, the semiconductor chip in the present invention is electrically connected to the outside.

Therefore, the present invention provides a semiconductor chip with switching voltage regulation and the ability to adapt to varying voltages demanded by various chip designs, which decreases transient response time, circuit routing area used on the PCB, and the complexity of circuit connection. These improvements lead to a decrease in the overall cost of manufacturing semiconductor devices.

To enable the objectives, technical contents, characteristics, and accomplishments of the present invention and the embodiments of the present invention are to be described in detail in reference to the attached drawings below.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows the structure of prior voltage regulating circuits.

FIG. **2** is a graph showing the relationship between the load current frequency of the circuit structure and output impedance.

FIG. **3** shows Embodiment 1 of the circuit of a prior step-down voltage regulator.

FIG. **4** shows Embodiment 2 of the circuit of a prior step-down voltage regulator.

FIG. **5** shows the corresponding circuit diagram of the present invention.

FIG. **6** is a graph showing the relationship between usage frequency and output impedance.

FIG. **7** shows the semiconductor chip of Embodiment 1.

FIGS. **7***a* to **7***e* show the processes of the semiconductor chip of Embodiment 1.

FIG. **8** shows the semiconductor chip of Embodiment 2.

FIGS. **8***a* to **8***u* and FIGS. **8***aa* to **8***am* show the processes of the semiconductor chip of Embodiment 2.

FIG. **9** shows the semiconductor chip of Embodiment 3.

FIGS. **9***a* to **9***d* show the processes of the semiconductor chip of Embodiment 3.

FIG. **10** shows the semiconductor chip of Embodiment 4.

FIGS. **10***a* to **10***i* show the processes of the semiconductor chip of Embodiment 4.

FIG. **11***a* shows the semiconductor chip of Embodiment 5.

FIG. **11***b* shows the semiconductor chip of Embodiment 6.

FIGS. **12** to **15** show the ball grid array (BGA) packaging structure of Embodiment 4.

FIGS. **16***a* to **16***c* show the packaging structure of the semiconductor chip of Embodiment 1, Embodiment 2, Embodiment 4, and Embodiment 5 in the present invention.

FIGS. **16***d* to **16***f* show the packaging structure of the semiconductor chip of Embodiment 6 in the present invention.

FIGS. **17***a* to **17***c* show the packaging structure of the semiconductor chip of Embodiment 3 in the present invention.

FIGS. **17***d* to **17***f* show the packaging structure of the semiconductor chip of Embodiment 6 in the present invention.

FIG. **18** is a view illustrating the equivalent circuit of the semiconductor chip of Embodiment 1 in the present invention.

FIG. **19** shows the equivalent circuit of the semiconductor chip of Embodiment 2 in the present invention.

FIG. **20** is a graph showing the relationship between voltage and time of the circuit in FIG. **19**.

FIG. **21***a* to **21***l* shows the manufacturing of the structure of Embodiment 7.

FIGS. **22***a* to **22***q* shows the manufacturing of the structure of Embodiment 8.

FIG. **23***a* to **23***b* shows the manufacturing of the structure of Embodiment 9 as seen from above.

FIG. **24***a* to **24***b* shows the structure of Embodiment 10.

FIG. **25***a* to **25***k* shows the manufacturing of the structure of Embodiment 11.

FIGS. **26** and **27** shows the circuit diagram of the present invention used as a voltage amplifying device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention discloses a semiconductor chip structure and its application circuit, wherein multiple passive devices are integrated on a semiconductor chip. By using active devices from semiconductor chips of different functions to match the passive components integrated on the semiconductor chip, immediate voltage adaptation can be achieved within a specific voltage range.

As opposed to the circuit structure disclosed in FIG. **1**, the present invention provides a semiconductor chip structure with the equivalent circuit structure shown in FIG. **5**. The most defining characteristic of the circuit structure used in the present invention is that the circuit structure contains the voltage regulator or called converter **12'** constructed after parasitic elements **14'** of PC board and parasitic elements **15'** of chip package, as opposed to circuit structures of FIG. **1** with voltage regulator **12'** before parasitic elements **14'** of PC board as in prior art. Therefore, because voltage regulator **12'** does not need to bear the burden of parasisitc elements **14'** and **15'**, the voltage regulator or converter integrated with a single chip allows circuit operation under higher frequency. [Also, this circuit structure design can lower manufacturing costs and simplify the routing design on the PCB because the distance between voltage regulator **12'** and corresponding electrical devices **16'** is shortened. The simplified routing design increases the speed and efficiency at which signals are delivered and solves the problem of large voltage fluctuations under high frequency usage. An example relationship between load current frequency and impedance resistance values are shown in FIG. **6**.

Following, the preferred embodiments of the each structure in the semiconductor chip structure will first be proposed. Then, in reference to specific embodiments, application circuits will be proposed.

Embodiment 1

In reference to FIG. **7**, substrate **100** is a type of semiconductor base. This substrate can be silicon based, gallium arsenide (GaAs) based, or silicon germanium (SiGe) based, and many of the devices, such as devices **110**, **112**, and **114**, are located in or over substrate **100**. These devices **110**, **112**, and **114** are all active devices mainly. Active devices include voltage feedback devices, switch controller, or MOS devices, such as p-channel MOS devices, n-channel MOS devices, BiCMOS devices, Bipolar Junction Transistor (BJT), or CMOS.

There is a thin circuit structure located on substrate **100**. This circuit structure includes a first dielectric layer **150**, multiple metal layers **140**, at least one second dielectric layer **155**. The thicknesses of the first dielectric layer **150** and second dielectric layer **155** are between 0.3 micrometers and 2.5 micrometers, and the materials that are used to make the first and second dielectric layers include boron containing silicate glass, silicon-nitride, silicon-oxide, silicon-oxynitride, and carbon containing low-k dielectric material. On the other hand, the thicknesses of metal layers **140** are between 0.1 micrometers and 2 micrometers, and the materials used to make the metal layers comprise copper layer, aluminum-copper alloy, tantalum, tantalum nitride, tungsten, and tungsten alloy. Devices **110**, **112**, **114** are electrically connected to metal layers **140** through a metal contact **120** and metal via **130**, which passes through first dielectric layer **150** and second dielectric layer **155**. Metal contact **120** and via **130** can be a W-plug or Cu-plug. In addition, the metal layers **140** are formed by various methods including damascene process, electroplating, CVD, and sputtering. For example, the damascene process, electroplating, sputtering, and CVD can be used to form copper metal layers **140**, or sputtering can be used to form aluminum metal layers **140**. On the other hand, the first dielectric layer **150** and second dielectric layer **155** are usually formed by Chemical Vapor Deposition (CVD).

Passivation layer **160** is over the circuit structure comprising the first dielectric layer **150**, metal layers **140**, and second dielectric layer **155**. This passivation layer **160** can protect devices **110**, **112**, **114** and the metal layers **140** described above from humidity and metal ion contamination. In other words, passivation layer **160** can prevent movable ions, such as sodium ions, moisture, transition metal ions, such as gold, silver, and copper, and other impurities from passing through and damaging devices **110**, **112**, **144**, which could be MOS devices, transistors, voltage feedback devices, and switch controller, or all of metal layers **140** that are below passivation layer **160**. In addition, passivation layer **160** usually consists of silicon-oxide (such as SiO_2), phosphosilicate glass (PSG), silicon-nitride (such as Si_3N_4) or silicon oxynitride. Passivation layer **160** typically has a thickness between 0.3 micrometers and 2 micrometers, and when it includes a silicon-nitride layer, this silicon-nitride layer usually has a thickness exceeding 0.3 micrometers and less than 2 micrometers.

There are currently ten methods of manufacturing passivation layer **160**.

In a first method, the passivation layer **160** is formed by depositing a silicon oxide layer with a thickness of between 0.2 and 1.2 μm using a CVD method and on the silicon oxide layer depositing a silicon nitride layer with thickness between 0.3 and 1.2 μm by using a CVD method.

In a second method, the passivation layer **160** is formed by depositing a silicon oxide layer with a thickness of between 0.2 and 1.2 μm using a CVD method, next depositing a silicon oxynitride layer with a thickness of between 0.05 and 0.3 μm on the silicon oxide layer using a Plasma Enhanced CVD (PECVD) method, and then depositing a silicon nitride layer with a thickness of between 0.2 and 1.2 μm on the silicon oxynitride layer using a CVD method.

In a third method, the passivation layer **160** is formed by depositing a silicon oxynitride layer with a thickness of between 0.05 and 0.3 μm using a CVD method, next depositing a silicon oxide layer with a thickness of between 0.2 and 1.2 μm on the silicon oxynitride layer using a CVD method, and then depositing a silicon nitride layer with a thickness of between 0.2 and 1.2 μm on the silicon oxide layer using a CVD method.

In a fourth method, the passivation layer **160** is formed by depositing a first silicon oxide layer with a thickness of between 0.2 and 0.5 μm using a CVD method, next depositing a second silicon oxide layer with a thickness of between 0.5 and 1 μm on the first silicon oxide layer using a spin-coating method, next depositing a third silicon oxide layer with a thickness of between 0.2 and 0.5 μm on the second silicon oxide layer using a CVD method, and then depositing a silicon nitride layer with a thickness of 0.2 and 1.2 μm on the third silicon oxide using a CVD method.

In a fifth method, the passivation layer **160** is formed by depositing a silicon oxide layer with a thickness of between 0.5 and 2 μm using a High Density Plasma CVD (HDP—

CVD) method and then depositing a silicon nitride layer with a thickness of 0.2 and 1.2 μm on the silicon oxide layer using a CVD method.

In a sixth method, the passivation layer **160** is formed by depositing an Undoped Silicate Glass (USG) layer with a thickness of between 0.2 and 3 μm, next depositing an insulating layer of TEOS, PSG or BPSG (borophosphosilicate glass) with a thickness of between 0.5 and 3 μm on the USG layer, and then depositing a silicon nitride layer with a thickness of 0.2 and 1.2 μm on the insulating layer using a CVD method.

In a seventh method, the passivation layer **160** is formed by optionally depositing a first silicon oxynitride layer with a thickness of between 0.05 and 0.3 μm using a CVD method, next depositing a silicon oxide layer with a thickness of between 0.2 and 1.2 μm on the first silicon oxynitride layer using a CVD method, next optionally depositing a second silicon oxynitride layer with a thickness of between 0.05 and 0.3 μm on the silicon oxide layer using a CVD method, next depositing a silicon nitride layer with a thickness of between 0.2 and 1.2 μm on the second silicon oxynitride layer or on the silicon oxide using a CVD method, next optionally depositing a third silicon oxynitride layer with a thickness of between 0.05 and 0.3 μm on the silicon nitride layer using a CVD method, and then depositing a silicon oxide layer with a thickness of between 0.2 and 1.2 μm on the third silicon oxynitride layer or on the silicon nitride layer using a CVD method.

In a eighth method, the passivation layer **160** is formed by depositing a first silicon oxide layer with a thickness of between 0.2 and 1.2 μm using a CVD method, next depositing a second silicon oxide layer with a thickness of between 0.5 and 1 μm on the first silicon oxide layer using a spin-coating method, next depositing a third silicon oxide layer with a thickness of between 0.2 and 1.2 μm on the second silicon oxide layer using a CVD method, next depositing a silicon nitride layer with a thickness of between 0.2 and 1.2 μm on the third silicon oxide layer using a CVD method, and then depositing a fourth silicon oxide layer with a thickness of between 0.2 and 1.2 μm on the silicon nitride layer using a CVD method.

In a ninth method, the passivation layer **160** is formed by depositing a first silicon oxide layer with a thickness of between 0.5 and 2 μm using a HDP—CVD method, next depositing a silicon nitride layer with a thickness of between 0.2 and 1.2 μm on the first silicon oxide layer using a CVD method, and then depositing a second silicon oxide layer with a thickness of between 0.5 and 2 μm on the silicon nitride using a HDP—CVD method.

In a tenth method, the passivation layer **160** is formed by depositing a first silicon nitride layer with a thickness of between 0.2 and 1.2 μm using a CVD method, next depositing a silicon oxide layer with a thickness of between 0.2 and 1.2 μm on the first silicon nitride layer using a CVD method, and then depositing a second silicon nitride layer with a thickness of between 0.2 and 1.2 μm on the silicon oxide layer using a CVD method.

In passivation layer **160**, there are more than one passivation layer openings **165**, which therefore expose part of the metal layers **140** below. The passivation layer openings **165** can be in the shape of a circle, square, rectangle, or polygon with more than five edges. Corresponding to different shapes, there are different definitions for opening dimensions. For example, a circle opening has dimensions defined by its diameter, a square opening has dimensions defined by its side length, and a polygon with more than five edges has dimensions defined by the longest diagonal.

The portion of the metal layers **140** exposed by the passivation layer openings **165** in the passivation layer **160** is defined to be pad **166**. On pad **166**, there can be an optional metal cap (not shown in figure) to protect pad **166** from being damaged by oxidation. This metal cap can be an aluminum-copper alloy, a gold layer, a titanium tungsten alloy layer, a tantalum layer, a tantalum nitride layer, or a nickel layer. For example, when pad **166** is a copper pad, there needs to be a metal cap, such as an aluminum-copper alloy, to protect the copper pad exposed by the passivation layer openings **165** from oxidation, which could damage the copper pad. Also, when the metal cap is an aluminum-copper alloy, a barrier layer is formed between the copper pad and aluminum-copper alloy. This barrier layer includes titanium, titanium tungsten alloy, titanium nitride, tantalum, tantalum nitride, chromium, or nickel. The following method is under a condition where there is no metal cap, but those familiar with such technology should be able to deduce a similar method with the addition of a metal cap.

Next, an under bump metal structure **250** is constructed over passivation layer opening **165**. The thickness of under bump metal structure **250** is between one micrometer and 15 micrometers. This under bump metal structure **250** is connected to external devices **310** and **320** through a solder layer **300**. The solder layer **300** may include gold-tin alloy, tin-silver alloy, tin-silver-copper alloy, or other lead-free alloy. Using tin-silver alloy as an example, the tin to silver ratio can be adjusted according to needs, with the most common tin/silver ratio being 96.0~97/3.0~4. The thickness of said solder layer **300** is between 30 micrometers and 350 micrometers.

Under bump metal structure **250** can be a TiW/Cu/Ni metal layer structure, Ti/Cu/Ni metal structure, Ti/Cu metal structure, or Ti/Cu/Ni/Au metal structure.

Referring to FIG. 7*a* to FIG. 7*e*, a method for forming the TiW/Cu/Ni/Au under bump metal structure **250** is first using the sputtering process or evaporating process to form a TiW adhesion/barrier metal layer **168** with thickness between 0.05 and 0.5 micrometers on pad **166** and passivation layer **160**, then using the sputtering process to form a copper seed layer **170** with thickness between 0.05 and 1 micrometer on TiW metal layer **168**. Next, a patterned photoresist layer **172** is formed on seed layer **170**. This patterned photoresist layer **172** has more than one opening **172*a*** revealing seed layer **170**. Next, using the electroplating or electroless plating process, copper metal layer **174** with thickness between 3 and 30 micrometers, nickel layer **176** with thickness between 0.5 and 5 micrometers, and gold layer **178** with thickness between 0.05 and 1.5 micrometer, preferred between 0.05 and 0.2 micrometers are formed respectively in opening **172*a*** of patterned photoresist layer **172**. Finally, photoresist layer **172**, the portions of seed layer **170** and TiW metal layer **168** that are not under gold layer **178** are removed, completing the TiW/Cu/Ni/Au under bump metal structure **250**. Here, Cu seed layer **170** removing process can be done by using wet etching solution containing H2SO4 or NH4OH, and TiW adhesion/barrier metal layer **168** removing process can be done by using wet etching solution containing 20~40% H2O2. It is preferred that the PH value of the etching solution for TiW removal is higher than 6 to prevent Cu corrosion during TiW removal.

Another ways to form seed layer **170** are an evaporating method, an electroplating method, or an electroless plating method, but preferred by a sputtering. Because seed layer **170** is important for the construction of electrical circuits thereon, the material used for seed layer **170** will vary according to material used for electrical circuits in following processes. For example, if the metal layer **174** made of copper material is formed on seed layer **170** by electroplating, then copper is also the optimal material to use for seed layer **170**. Similarly, if the metal layer **174** made of gold material is formed on seed layer **170** by electroplating then gold is the optimal material to use for seed layer **170**.

If the metal layer **174** made of palladium material is formed on seed layer **170** by electroplating, then palladium is also the optimal material to use for seed layer **170**. If the metal layer **174** made of platinum material is formed on seed layer **170** by electroplating, then platinum is also the optimal material to use for seed layer **170**. If the metal layer **174** made of rhodium material is formed on seed layer **170** by electroplating, then rhodium is also the optimal material to use for seed layer **170**. If the metal layer **174** made of ruthenium material is formed on seed layer **170** by electroplating, then ruthenium is also the optimal material to use for seed layer **170**. If the metal layer **174** made of rhenium material is formed on seed layer **170** by electroplating, then rhenium is also the optimal material to use for seed layer **170**. If the metal layer **174** made of silver material is formed on seed layer **170** by electroplating, then silver is also the optimal material to use for seed layer **170**.

The structure of under bump metal structure **250** will vary depending on the method use to form solder layer **300**:

For example, if solder layer **300** is formed on under bump metal structure **250** by an electroplating method, the under bump metal structure **250** is preferred to be a TiW/Cu/Ni alloy structure or Ti/Cu/Ni alloy structure, with the solder structure **300** electroplated on the nickel layer, the TiW or Ti metal layer, formed by a sputtering method, on pad **166** and passivation layer **160**, and Cu/Ni deposited by electroplating. In between the TiW or Ti metal layer and copper layer, there is a copper seed layer deposited by sputtering.

In another example, if the solder layer **300** is provided by external devices **300** and **320** or solder printing, then the under bump metal structure **250** is preferred to be a TiW/Cu/Ni/Au or Ti/Cu/Ni/Au structure.

Through solder layer **300**, the under bump metal structure **250** on passivation layer opening **165** is electrically connected to external devices **310** and **320** (labeled as **310** in figure). External devices **310** and **320** are also electrically connected to the metal layer **140** below passivation layer **165**, therefore external devices **310** and **320** to also be electrically connected to devices **110**, **112**, and **114**.

External devices **310** and **320** are passive devices, which include inductors, capacitors, or integrated passive devices. In the present invention, external devices **310** and **320** are a capacitor and an inductor, respectively. For example, external device **310** may be a capacitor, while external device **320** may be an inductor, or external device **310** may be an integrated passive device, while external device **320** may be an inductor. The dimensions of external devices **310** and **320** may be chosen from industrial standard dimension 1210, dimension 0603, dimension 0402, or dimension 0201, wherein said dimension 0201 stands for 0.02 inches by 0.01 inches, and dimension 1210, dimension 0603, and dimension 0402 deduced by the same standard. In general, external devices **310** and **320** have a length between 0.2 mm and 5 mm and a width between 0.1 mm and 4 mm. External devices **310** and **320** are directly constructed on under bump metal structure **250** through the connection of solder layer **300**.

Also, external devices **310** and **320** can be mounted either before or after a dice sawing procedure is performed on substrate **100**.

Finally, the semiconductor chip after dice sawing procedures as disclosed in Embodiment 1 can be electrically connected to external circuits or power supplies through wires made by wire-bonding or through solder by flip chip techniques.

Embodiment 2

Referring to FIG. **8**, the structure of Embodiment 2 is similar to that of Embodiment 1, and therefore an explanation of some of the manufacturing process and properties will not be repeated. The difference between Embodiment 2 and Embodiment 1 lies in an under bump metal structure **260** and a bonding metal layer **400***c* that are constructed on or over pad **166***b*. Said bonding metal layer **400***c* can be used to connect electrically to external circuits through a wire formed by wire-bonding (not shown in figure).

The structure of Embodiment 2 can be manufactured with the following methods:

Manufacturing method 1 of Embodiment 2:

Referring to FIG. **8***a*, integrated circuit **20** represents all structures below passivation layer **160**. Also included in integrated circuit **20** are substrate **100**, devices **110**, **112**, **114**, first dielectric layer **150**, metal layers **140**, second dielectric layer **155**, metal contact **120**, and via **130**, wherein multiple passivation layer openings **165** reveal multiple pads **166***a* and **166***b*.

Referring to FIG. **8***b*, an adhesion/barrier layer **22** is formed on passivation layer **160** and pad **166***a* and **166***b* by using sputtering. The thickness of adhesion/barrier layer **22** is between 0.1 micrometers and 1 micrometer, with an optimal thickness between 0.3 micrometers and 0.8 micrometers. The adhesion/barrier can be selected from or composed of the following materials, Ti, TiW, TiN, Ta, TaN, Cr, and Mo. Ti and TiW are the two preferred materials for adhesion/barrier.

Referring to FIG. **8***c*, a seed layer **24** with a thickness between 0.05 micrometers and 1 micrometer (and an optimal thickness between 0.1 micrometers and 0.7 micrometers) is then formed on adhesion/barrier layer **22**. Similar to seed layer **170** described above, the material used for seed layer **24** will vary according to the material of metal layers formed later. The material of seed layer can be Cu, Au or Ag. Au is the preferred seed layer material in this embodiment.

Referring to FIG. **8***d*, photoresist layer **26** is formed on seed layer **24**, and through spin coating, exposure and development, photoresist layer **26** is patterned, forming multiple photoresist layer openings **26***a* in photoresist layer **26**, which reveal portions of seed layer **24** that are over pad **166***b*.

Referring to FIG. **8***e*, bonding metal layer **400***c* is formed by an electroplating method on seed layer **24**, which is in photoresist layer opening **26***a*. The bonding metal layer **400***c* consists of materials such as gold, copper, silver, palladium, rhodium, ruthenium, rhenium, or nickel, and may have a single metal layer structure or multiple metal layer structure. The thickness of bonding metal layer **400***c* is between 1 micrometers and 100 micrometers, with optimal thickness between 1.5 micrometers and 15 micrometers. The bonding metal layer **400***c* may be composed with combinations of the multiple metal layer structure which comprise Cu/Ni/Au, Cu/Au, Cu/Ni/Pd, and Cu/Ni/Pt. In this embodiment, bonding metal layer **400***c* is preferred to be a single layer made of gold.

Referring to FIG. **8***f*, remove patterned photoresist **26** and portions of seed layer **24** that are not below metal layer **400***c*. If seed layer **24** is made of gold, seed layer **24** is removed by using solution containing I_2 and KI.

Referring to FIG. **8***g*, a seed layer **28** with a thickness between 0.05 micrometers and 1 micrometer (and an optimal thickness between 0.1 micrometers and 0.7 micrometers) is formed on adhesive/barrier layer **22** and metal layer **400***c*. In this embodiment, the material of said seed layer **28** is preferred to be copper (Cu). Similar to seed layer **170** described above, the material used for seed layer **28** will vary according to the material of metal layers formed later.

Referring to FIG. **8***h*, a photoresist layer **30** is formed on seed layer **28**, and through spin coating, exposure and development, photoresist layer **30** is patterned, forming multiple photoresist layer openings **30***a* in photoresist layer **30**, which reveal portions of seed layer **28** that are over pad **166***a*.

Referring to FIG. **8***i*, a metal layer **32** is formed by an electroplating method on seed layer **28**, which is in photoresist layer opening **30***a*. The metal layer **32** is made of copper, and has a thickness between 1 micrometer and 100 micrometers, with optimal thickness between 1.5 micrometers and 15 micrometers.

Referring to FIG. **8***j*, a metal layer **34** is formed by an electroplating method on metal layer **32**, which is in photoresist layer opening **30***a*. The metal layer **34** is made of nickel, and has a thickness between 0.1 micrometers and 20 micrometers, with optimal thickness between 1 micrometer and 5 micrometers.

Referring to FIG. **8***k*, a metal layer **300** is formed by an electroplating method on metal layer **34**, which is in photoresist layer opening **30***a*. The metal layer **300** consists of material such as tin, Sn/Ag alloy, Sn/In alloy, Sn/Ag/Cu alloy, and any other lead free soldering material, and has a thickness between 5 micrometers and 300 micrometers, with optimal thickness between 20 micrometers and 150 micrometers.

Referring to FIG. **8***l*, remove patterned photoresist layer **30** and the portions of seed layer **28** and adhesive/barrier layer **22** that are not below metal layer **300**. To remove seed layer **28** made of copper, NH_3^+ or SO_4^{2+} is used to etch the copper. And to remove adhesive/barrier layer **22**, dry etching or wet etching can be used. Dry etching involves using reactive ion etching or Argon sputter etching. On the other hand, when using wet etching, if adhesive/barrier layer **22** is made of Ti/W alloy, hydrogen peroxide can be used to remove the layer, and if adhesion/barrier layer **22** is made of Ti, HF containing solution can be used to remove the layer. Meanwhile, the multiple metal layers, such as metal layer **34**, metal layer **32**, seed layer **28**, and adhesive/barrier layer **22**, below metal layer **300** are the under bump metal structure **250** shown in FIG. **8** and the seed layer **28** and adhesion/barrier layer **24** below metal layer **400***c* are the under bump metal structure **260** show in FIG. **8** respectively. In the manufacturing of this embodiment, under bump metal structure **250** is a TiW/Cu/Ni structure, and under bump metal structure **260** is a TiW/Au seed layer.

Referring to FIG. **8***m*, solder layer **300** collates into a semi-sphere through the process of reflow in an environment containing oxygen less than 20 ppm.

Referring to FIG. **8***n*, mount external device **310** and external device **320** separately on solder layer **300**. In this embodiment, external devices **310** and **320** are passive devices, which include inductors, capacitors, or integrated passive devices. In the present invention, external devices **310** and **320** are two different passive devices. For example, external device **310** may be a capacitor, while external device **320** may be an inductor, or external device **310** may be an integrated passive device, while external device **320** may be an inductor. External devices **310** and **320** each have multiple contact points (not shown in figure). On the surface of these multiple contact points, there are metals suited for mounting on metal layer **300**. For example, the surface of contact points may have a soldering material layer such as tin containing layer or a solder wetting layer such as gold layer.

The dimensions of external devices **310** and **320** may be chosen from industrial standard dimension 1210, dimension 0603, dimension 0402, or dimension 0201, wherein said dimension 0201 stands for 0.02 inches by 0.01 inches, and dimension 1210, dimension 0603, and dimension 0402 deduced with the same standard. In general, external devices **310** and **320** have a length between 0.2 mm and 5 mm, a width between 0.1 mm and 4 mm, and a height between 0.01 mm and 2 mm.

The next steps will be a dicing procedure, where substrate **100** is first i sawed into multiple chips. Next, a wire **37** is formed by wire-bonding on metal layer **400***c*, which is on pad **166***b*, and said wire **37** is used to connect to external circuits or power supplies.

Also, external devices **310** and **320** can be mounted after dicing procedures are performed on substrate **100**.

Manufacturing method 2 of Embodiment 2:

Manufacturing method 2 differs from manufacturing method 1 in that solder layer **300** is provided by external devices **310** and **320** or external adding during mounting process of device **310** and **320**. In other words, before mounting with external devices **310** and **320**, the structure does not have a solder layer **300** on the under bump metal structure **250**. The following is a detailed description of the manufacturing process.

Continuing from FIG. **8***b* and referring to also FIG. **8***o*, a seed layer **38** is formed on adhesive/barrier layer **22** with a thickness between 0.05 micrometers and 1 micrometers (and an optimal thickness between 0.1 micrometers and 0.7 micrometers. In this embodiments, seed layer **38** is made of Cu. Similar to seed layer **170** described above, the material used for seed layer **38** will vary according to the material of metal layers formed later.

Referring to FIG. **8***p*, photoresist layer **40** is formed on seed layer **38**, and through spin coating, exposure and development, photoresist layer **40** is patterned, forming multiple photoresist layer openings **40***a* in photoresist layer **40**, which separately reveal portions of seed layer **24** that are over pad **166***b* and pad **166***a*.

Referring to FIG. **8***q*, metal layer **42** is formed by an electroplating method on seed layer **38**, which is in photoresist layer opening **40***a*. The metal layer **42** consists of materials such as gold, copper, silver, palladium, rhodium, ruthenium, rhenium, or nickel, and may have a single metal layer structure or multiple metal layer structure. The thickness of metal layer **42** is between 1 micrometers and 100 micrometers, with optimal thickness between 1.5 micrometers and 15 micrometers. In this embodiment, metal layer **42** is made of copper.

Referring to FIG. **8***r*, a metal layer **44** is formed by an electroplating method on metal layer **42**, which is in photoresist layer opening **40***a*. The metal layer **44** is made of nickel, and has a thickness between 0.5 micrometers and 100 micrometers, with optimal thickness between 1 micrometer and 5 micrometers.

Referring to FIG. **8***s*, a metal layer **46** is formed by an electroplating or electroless-plating method on metal layer **44**, which is in photoresist layer opening **40***a*. The metal layer **46** consists of materials such as gold, silver, palladium, rhodium, ruthenium, or rhenium, and has a thickness between 0.03 micrometers and 2 micrometers, with optimal thickness between 0.05 micrometer and 0.5 micrometers. In this embodiment, the material of metal layer **46** is gold (Au).

Referring to FIG. **8***t*, remove patterned photoresist layer **40** and the portions of seed layer **44** and adhesive/barrier layer **22** that are not below metal layer **46**. To remove seed layer **24** made of copper, a NH_3^+ or SI_4^{2+} containing solution is used to etch the copper. To remove adhesive/barrier layer **22**, dry etching or wet etching can be used. Dry etching involves using reactive ion etching or Argon sputter etching. On the other hand, when using wet etching, if adhesive/barrier layer **22** is made of Ti/W alloy, hydrogen peroxide can be used to remove the layer, and if adhesion/barrier layer **22** is made of Ti, HF containing solution can be used to remove the layer.

Referring to FIG. **8***u*, connect external device **310** and external device **320** separately on solder layer **300**. The external devices **310** and **320** contain a solder layer **300**, or forming a solder layer **300** on metal layer **46** by screen printing method, and through this solder layer **300**, external devices **310** and **320** are mounted to metal layer **46**.

In this embodiment, external devices **310** and **320** are passive devices, which include inductors, capacitors, or integrated passive devices. In the present invention, external devices **310** and **320** are two different passive devices. For example, external device **310** may be a capacitor, while external device **320** may be an inductor, or external device **310** may be an integrated passive device, while external device **320** may be an inductor. External devices **310** and **320** each have multiple contact points (not shown in figure). On the surface of these multiple contact points, there are metals suited for mounting on metal layer **300**. For example, the surface of contact points may have a soldering material layer or a solder wetting layer such as gold layer.

The dimensions of external devices **310** and **320** may be chosen from industrial standard dimension 1210, dimension 0603, dimension 0402, or dimension 0201, wherein said dimension 0201 stands for 0.02 inches by 0.01 inches, and dimension 1210, dimension 0603, and dimension 0402 deduced with the same standard. In general, external devices **310** and **320** have a length between 0.2 mm and 5 mm, a width between 0.1 mm and 4 mm, and a height between 0.01 mm and 2 mm.

The next step is a dicing procedure, where substrate **100** is sawed into multiple chips. Then, a wire **47** is conducted by wire-bonding on metal layer **46**, which is on pad **166***b*, and said wire **47** is used to connect to outside circuits or power supplies.

Also, external devices **310** and **320** can be mounted after dicing procedures are performed on substrate **100**.

Manufacturing method and structure 3 of Embodiment 2:

Referring to FIG. **8***aa* and FIG. **8***ab*, FIGS. **8***aa* is a cross-sectional view cut along the line **2**-**2** in FIG. **8***ab*. Integrated circuit **20** represents all structures below passivation layer **160**. Also included in integrated circuit **20** is substrate **100**, devices **110**, **112**, **114**, first dielectric layer **150**, metal layers **140**, second dielectric layer **155**, metal contact **120**, and via **130**, wherein multiple passivation layer openings **165***a* and openings **165***b* in passivation layer **160** reveal multiple pads **166***a*, pads **166***b* and **166***ab*. Multiple metal pads **166***a* and **166***b* are designed in a rectangle preferentially.

Referring to FIG. **8***ac*, an adhesion/barrier layer **22** is formed on passivation layer **160**, pad **166***a* and **166***b* and **166***b* by using sputtering method. The thickness of adhesion/barrier layer **22** is between 0.1 micrometers and 1 micrometer, with an optimal thickness between 0.3 micrometers and 0.8 micrometers. The adhesion/barrier can be selected from or composed of the following materials, Ti, TiW, TiN, Ta, TaN, Cr, and Mo. Ti and/or TiW are the preferred material for adhesion/barrier.

Referring to FIG. **8***ad*, a seed layer **38** with a thickness between 0.05 micrometers and 1 micrometers (and an optimal thickness between 0.1 micrometers and 0.7 micrometers) is then formed on adhesion/barrier layer **22**. Similar to seed layer **170** described above, the material used for seed layer **38** will vary according to the material of metal layers formed later. The material of seed layer **38** can be Cu, Au or Ag. Cu is the preferred seed layer material in this embodiment.

Referring to FIG. **8***ae*, photoresist layer **40** is formed on seed layer **38**, and through spin coating, exposure and development, photoresist layer **40** is patterned, forming multiple photoresist layer openings **40***a* in photoresist layer **40**, which separately reveal portions of seed layer **38** that are over pad **166***a* and pad **166***b*.

Referring to FIG. **8***af*, metal layer **42** is formed by an electroplating method on seed layer **38**, which is in photoresist layer opening **40***a*. The metal layer **42** consists of materials such as gold, copper, silver, palladium, rhodium, ruthenium, or rhenium. The thickness of metal layer **42** is between 1 micrometers and 100 micrometers, with optimal thickness between 1.5 micrometers and 15 micrometers. In this embodiment, metal layer **42** is preferred to be a single layer made of copper.

Referring to FIG. **8***ag*, metal layer **44** is formed by an electroplating method on metal layer **42**, which is in photoresist layer opening **40***a*. The metal layer **44** consists of nickel preferentially. The thickness of metal layer **44** is between 0.1 micrometers and 10 micrometers, with optimal thickness between 0.5 micrometers and 5 micrometers.

Referring to FIG. **8***ah*, metal layer **46** is formed by an electroplating method on metal layer **44**, which is in photoresist layer opening **40***a*. The metal layer **46** consists of materials such as gold, copper, silver, palladium, rhodium, ruthenium, or rhenium. The thickness of metal layer **46** is between 0.03 micrometers and 5 micrometers, with optimal thickness between 0.05 micrometers and 1.5 micrometers. In this embodiment, metal layer **46** is preferred to be a single layer made of gold.

Referring to FIG. **8***ai*, remove patterned photoresist layer **40** and the portions of seed layer **38** and adhesive/barrier layer **22** that are not below metal layer **46**. To remove seed layer **38** made of copper, NH_3^+ or SO_4^{2+} containing solution is used to etch the copper. To remove adhesive/barrier layer **22**, dry etching or wet etching can be used. Dry etching involves using reactive ion etching or Argon sputter etching. On the other hand, when using wet etching, if adhesive/barrier layer **22** is made of Ti/W alloy, hydrogen peroxide can be used to remove the layer, and if adhesion/barrier layer **22** is made of Ti, HF containing solution can be used to remove the layer.

Referring to FIG. **8***aj*, connect external device **310** on the metal layer **46**, which is over the pads **166***a*. The external devices **310** have a solder layer **300**, or forming a solder layer **300** on metal layer **46** by screen printing, and through this solder layer **300**, external devices **310** are mounted on metal layer **46**.

Referring to FIG. **8***ak* and FIG. **8***al*, FIGS. **8***al* is a cross-sectional view cut along the line **2**-**2'** in FIG. **8***ak*. Connect external device **320** on the metal layer **46**, which is over the pads **166***ab* and the external device **320** is also over the external device **310**. The external devices **320** have a solder layer **301**, or forming a solder layer **301** on metal layer **46** by screen printing, and through this solder layer **301**, external devices **320** are mounted on metal layer **46**.

Referring to FIG. **8***am*, perform a dicing process to singular each chip, where substrate **100** is sawed into multiple chips. Next, a wire **47** is formed by wire-bonding on metal layer **46**, which is on pad **166***b*, and said wire **47** is used to connect to outside circuits or power supplies.

Also, external devices **310** and **320** can be mounted after dicing procedures are performed on substrate **100**.

Embodiment 3

Referring to FIG. **9**, Embodiment 3 is similar to Embodiment 2, with the difference being the material and thickness of connecting metal layer **400**. In Embodiment 3, solder layer **400** is constructed on pad **166***a* and **166***b*. The following is a description of the formation of the structure of Embodiment 3.

Manufacturing method of Embodiment 3:

Embodiment 3 can continue from FIG. **8***r* of manufacturing method 2 of Embodiment 2. Referring to FIG. **9***a*, a solder layer **400** is formed on metal layer **44** in photoresist layer opening **40***a* by an electroplating method. The thickness of solder layer **400** is between 30 micrometers and 350 micrometers. Chosen materials of solder layer **400** include tin/silver, tin/copper/silver, and tin/lead alloy.

Referring to FIG. **9***b*, remove patterned photoresist layer **40** and the portions of seed layer **38** and adhesive/barrier layer **22** that are not below solder layer **400**. To remove seed layer **38** made of copper, NH_3^+ or SO_4^{2+} containing solution is used to etch the copper.

Referring to FIG. **9***c*, use a reflow process as previous description for FIG. **8***m* so that solder layer **400** will reach melting point and aggregate into a semi-spherical shape.

Referring to FIG. **9***d*, external device **310** and external device **320** are separately mounted to solder layer **400** over pad **166***a*. In this embodiment, external devices **310** and **320** are passive devices, which include inductors, capacitors, and integrated passive devices. In the present invention, external devices **310** and **320** are two different passive devices. For example, external device **310** may be a capacitor, while external device **320** may be an inductor, or external device **310** may be an integrated passive device, while external device **320** may be an inductor.

The dimensions of external devices **310** and **320** may be chosen from industrial standard dimension 1210, dimension 0603, dimension 0402, or dimension 0201, wherein said dimension 0201 stands for 0.02 inches by 0.01 inches, and dimension 1210, dimension 0603, and dimension 0402 deduced by the same standard. In general, external devices **310** and **320** have a length between 0.2 mm and 5 mm, a width between 0.1 mm and 4 mm, and a height between 0.01 mm and 2 mm.

Embodiment 4

Referring then to FIG. **10**, in the semiconductor chip structure revealed by this embodiment, a first polymer layer **200** on passivation layer **160** can be optionally formed. Said first polymer layer **200** has a thickness between 3 micrometers and 25 micrometers and is made of materials such as polyimide (PI), benzocyclobutene (BCB), parylene, epoxy resins, elastomers, and porous dielectric material. The following is a description of the formation of the structure of Embodiment 3.

Manufacturing method of Embodiment 4:

Referring to FIG. **10***a*, integrated circuit **20** is used to represent various structures below passivation layer **160**. Integrated circuit **20** includes substrate **100**, devices **110**, **112**, **114**, first dielectric layer **150**, metal layers **140**, second dielectric layer **155**, metal contact **120**, and metal via **130**, wherein passivation layer **160** has multiple openings **165** that reveal multiple pads **166**.

Referring to FIG. **10***b*, a photosensitive polymer layer **200** with a thickness between 3 micrometers and 25 micrometers is formed on passivation layer **160**, and through spin coating, exposure and development, and O2 plasma ash or etching, polymer layer **200** is patterned, forming many openings **200***a* in polymer layer **200**. These openings **200***a* reveal pad **166**. Polymer layer **200** is then heated to a temperature between 150 and 390 degrees Celcius to cure polymer layer **200** so that said polymer layer **200** will harden. The material of polymer layer **200** can be chosen from polyimide (PI), benzocyclobutene (BCB), parylene, epoxy-based material, or ester type polymers, such as epoxy resins or photoepoxy SU-8 provided by Sotec Microsystems of Swiss Renens, or elastomers, such as silicone.

Referring to FIG. **10***c*, an adhesion/barrier layer **48** is formed on polymer layer **200** and pad **166** through a sputtering method. The thickness of the adhesion/barrier layer **48** is between 0.1 micrometer and 1 micrometer, with an optimal thickness between 0.2 micrometers and 0.5 micrometers. The material of adhesion/barrier layer **48** can be Ti, TiW, TiN, Ta, TaN or composite of the above metals.

Referring to FIG. **10***d*, a seed layer **50** with a thickness between 0.05 micrometers and 1 micrometers (optimal thickness between 0.08 micrometers and 0.5 micrometers) is formed on the adhesion/barrier layer. The material of said seed layer **50** in this embodiment is gold (Au), but as in the description of seed layer **170** above, the material of seed layer **50** will vary depending on the material of the metal layer formed later on.

Referring to FIG. **10***e*, a photoresist layer **52** is formed on seed layer **50**, and through spin coating, exposure and development a patterned photoresist layer **52** is formed, with multiple photoresist openings **52***a* on photoresist layer **52** that reveal seed layer **50** on pad **166**.

Referring to FIG. **10***f*, metal layer **220** is formed on seed layer **50** in photoresist layer opening **52***a* by an electroplating method. The material of metal layer **220** includes gold, copper, silver, palladium, platinum, rhodium, ruthenium, rhenium, or nickel, and may have a single metal layer structure or multiple metal layer structure. The thickness of metal layer **220** is between 2 micrometers and 25 micrometers, with optimal thickness between 3 micrometers and 10 micrometers. Furthermore, the structure of metal layer **220** with a multiple metal layer structure can include combinations such as Cu/Ni/Au, Cu/Au, Cu/Ni/Pd, and Cu/Ni/Pt. In this embodiment metal layer **220** is preferred a single gold layer.

Referring to FIG. **10***g*, remove patterned photoresist layer **52** and portions of seed layer **50** and adhesive/barrier layer **48** that are not below metal layer **220**. If seed layer **50** is made of gold, seed layer **50** is removed by using I_2 plus KI solution. On the other hand, hydrogen peroxide (H_2O_2) can be used to remove adhesive/barrier layer **48** if the material of the adhesion/barrier layer **48** is TiW. The portions of seed layer **50** and adhesive/barrier layer **48** under metal layer **220** correspond to label **210** in FIG. **10**.

Referring to FIG. **10***h*, a photosensitive polymer layer **230** with a thickness between 3 micrometers and 25 micrometers is formed. Through spin coating, exposure, development, and O2 plasma ash or etching, to form many openings **240***a* in polymer layer **230**, which expose metal layer **200**. Next, polymer layer **230** is heated and cured. This curing process proceeds at a temperature between 150 degrees Celsius and 380 degrees Celsius. The material of polymer layer **230** can be chosen from polyimide (PI), benzocyclobutene (BCB), parylene, epoxy-based material, or ester type polymers, such as epoxy resins or photoepoxy SU-8 provided by Sotec Microsystems of Swiss Renens, or elastomers, such as silicone.

Metal layer **220** revealed by openings **240***a* is defined to be multiple pads **220***a* and one wire bonding pad **220***b*. Pad **220***a* can be used to connect to external devices **310** and external device **320**, and wire binding pad **220***b* can be connected to external circuits or power supplies through wires formed by the wire bounding method. In this embodiment, external devices **310** and **320** are passive devices, which include, inductors, capacitors, and integrated passive devices. In the present invention, external devices **310** and **320** are two different passive devices. For example, external device **310** may be a capacitor, while external device **320** may be an inductor, or external device **310** may be an integrated passive device, while external device **320** may be an inductor.

The dimensions of external devices **310** and **320** may be chosen from industrial standard dimension 1210, dimension 0603, dimension 0402, or dimension 0201, wherein said dimension 0201 stands for 0.02 inches by 0.01 inches, and dimension 1210, dimension 0603, and dimension 0402 deduced by the same standard. In general, external devices **310** and **320** have a length between 0.2 mm and 5 mm, a width between 0.1 mm and 4 mm, and a height between 0.01 mm and 2 mm.

Referring to FIG. **10***i*, external device **310** and external device **320** are separately connected to pads **220***a*. External device **310** and external device **320** include a solder layer **400**, with a thickness between 30 micrometers and 350 micrometers, and made of materials such as Sn/Ag, Sn/Cu/Ag, Sn/Au alloy, or other related materials. The said solder layer **400** may be provided by screen printing process instead of included in external devices. External device **310** and external device **320** are connected to pads **220***a* through solder layer **400** by using surface mount technology.

The next step is a dicing procedure, where substrate **100** is sawed into multiple chips. Then a wire **56** is formed by wire bounding on wire bonding pad **220***b*, and said wire **56** is used to connect wire bonding pad **220***b* to external circuits or power supplies.

Also, external devices **310** and **320** can be mounted after dicing procedures are performed on substrate **100** by using surface mount technology.

Embodiment 5

Referring to FIG. **11***a*, the pad metal **166** of the circuit structure in above mentioned four embodiments is made of aluminum. However, in this fifth embodiment, the pad metal **166** is made of copper. When the pad metal **166** is made of copper, there needs to be a metal cap layer **170** to protect pad **166** revealed by passivation layer **160** openings, so that pad **166** will not be damaged by oxidation and can sustain later on processes such as wire bounding and flip-chip. The metal cap layer **170** is an aluminum-copper layer, a gold layer, a titanium (Ti) layer, a titanium tungsten alloy layer, a tantalum (Ta) layer, a tantalum nitride (TaN) layer, or a nickel (Ni) layer. When the metal cap is an aluminum-copper layer, a barrier layer (not shown in figure) is formed between the copper pad **166** and metal cap layer **170**. This barrier layer can be titanium, titanium tungsten alloy, titanium nitride, tantalum, tantalum nitride, chromium, or nickel.

The manufacturing of under bump metal structure and mounting external devices in FIG. **11***a* is the same as that of the embodiment 4.

Embodiment 6

Referring to FIG. **11***b*, the difference between Embodiment 6 and the first to fifth embodiments is that external devices are integrated into a single external device **330**. For example, external device **330** can be an integrated passive device of a capacitor and an inductor. Except for external device **330**, the manufacturing process and materials are all identical to those of the first to fifth embodiments. Therefore, the manufacturing process and materials of identical devices will not be repeated.

All the semiconductor chip structures described in the above six embodiments can be packaged in the Ball Grid Array (BGA) as shown in FIGS. **12** to **15**. FIGS. **12** to **15** reveal the packaging structure of a semiconductor chip package structure with only one semiconductor device. FIG. **12** explains one of the packaging structure of FIG. **7** of the Embodiment 1, FIG. **8** of Embodiment 2, FIG. **10** of Embodiment 4, and FIG. **11***a* of the Embodiment 5. The packaging structure of FIG. **12** includes electrically connecting the integrated circuit **20** to the BGA substrate **500** through wire **510**, and sealing the above mentioned devices with molding compound **520**. BGA substrate **500** has multiple solder balls **530** is electrically connected to outside circuits through these solder balls **530**.

On the other hand, FIG. **13** describes one of the packaging structures of FIG. **9** in Embodiment 3. The integrated circuit **20** is electrically connected to BGA substrate **500** through solder layer **400**. Then, the above mentioned devices are sealed with a molding compound **520**, and the BGA substrate **500** is electrically connected to outside circuits through solder balls **530**. Said molding compound **520** is a polymer such as epoxy resin or polyimide compound.

In FIG. **14** and FIG. **15**, the external device **310** and **320** in FIGS. **12** and **13** are replaced by an integrated passive device **330** (such as in embodiment 6). In FIG. **14**, the integrated circuit **20** is electrically connected to the BGA substrate **500** through wire **510**, and in FIG. **15**, it is electrically connected to the BGA substrate **500** through solder layer **400***a*.

Aside from above mentioned BGA packaging structure, the present invention can use common packaging form such as the Thin Small Outline Package (TSOP), Small Outline J-Lead (SOJ), s Quad Flat Package (QFP), Think Quad Flat Package (TQFP), or other common lead frame packaging form. As shown in FIG. **16***a* to **16***f* and FIG. **17***a* and **17***f*, the integrated circuit **20** is constructed on lead frame **600**, which is made of copper or copper alloy and has a thickness between 100 micrometers and 2000 micrometers.

FIG. **16***a* to **16***c* describe the packaging structure of FIG. **7** of Embodiment 1, FIG. **8** of Embodiment 2, FIG. **10** of Embodiment 4, and FIG. **11***a* of Embodiment 5. Integrated circuit **20** is electrically connected to lead frame **600** through wire **510**. The above mentioned devices are then sealed with a molding compound **520**, but exposing the leads of lead frame **600**. These leads are then connected to an outside circuit.

In FIGS. **16***d* to **16***f*, the external devices **310** and **320** in FIGS. **16***a* to **16***c* are replaced by an integrated device **330** (as in Embodiment 6).

In FIGS. **17***a* to **17***c* another packaging structure of FIG. **9** in Embodiment 3 is shown. Integrated circuit **20** is electrically connected to lead frame **600** through solder layer **400***b*, and the above-mentioned devices are then sealed with molding compound **520**, but exposing the leads of lead frame **600**. These leads are then connected to other outside circuits. Said molding compound **520** is a polymer such as epoxy resin or polyimide compound.

In FIGS. **17***d* to **17***f*, the external devices **310** and **320** in FIGS. **17***a* to **17***c* are replaced by an integrated device **330** (as in Embodiment 6).

The description up until this point has been of semiconductor chip structures. Following is the description and explanation of application circuits corresponding to the semiconductor chip structures. The application circuits include an internal circuit, an external circuit, and a metal connection which are all integrated on a single semiconductor chip.

In FIG. **18**, the simplified equivalent circuit shown is similar to the application circuit shown in FIG. **7**. Devices **112**, and **114** in FIG. **7** correspond respectively to, and voltage feedback device **1112**, and switch circuit including switch controller **1114***a* and switch MOS **1114***b*, **1114***e* in FIG. **18**, and external devices **320** and **310** in FIG. **7** correspond respectively to inductor **1320** and capacitor **1310** in FIG. **18**, wherein inductor **1320** and capacitor **1310** are connected and voltage feedback device **1112** is electrical connected between inductor **1320** and capacitor **1310**. This voltage feedback device **1112** can feedback the voltage signal between inductor **1320** and capacitor **1310**. In the circuit revealed by FIG. **18**, a power supply input **1311** uses wire-bonded leads or solder layers on contact pads of the semiconductor chip to input power to MOS **1114***b*, which is below the passivation layer of the semiconductor chip. Feedback device **1112** then takes the voltage signal passing between inductor **1320** and capacitor **1310**, and the voltage signal is transmitted back to switch controller **1114***a*. Switch controller **1114***a* then uses the signal to decide the on and off timing of the two MOS **1114***b* and **1114***e* located on the semiconductor chip, which allows switch controller **1114***a* to regulate the duty cycle of MOS **1114***b* and **1114***e* and therefore to regulate the voltage at output **1313**. In the present invention, inductor **1320**, capacitor **1310**, switch controller **1114***a*, and voltage feedback device **1112** form the voltage regulator or converter. Therefore, according to different working voltage ranges of semiconductor chips, voltage regulator integrated with the semiconductor chip can use the described mechanism to regulate voltages immediately, using the shortest transfer path to transfer power supply to the semiconductor chip, allowing the voltage level of the semiconductor chip's power supply to be quickly regulated to a specific voltage range.

Also, according to the electrical circuit structure shown in FIG. **18** and the semiconductor chip structure disclosed by the present invention, since the passive components in the present invention are all integrated over semiconductor substrates with active devices, therefore, multiple electronic devices could easily be connected to each other. FIG. **19** shows an equivalent circuit of multiple passive devices and a semiconductor chip connected together, wherein all switch MOS **1114***f*, **1114***h*, **1114***j*, **1114***g*, **1114***i*, **1114***k* and inductor **1320***a*, **1320***b*, and **1320***c* connect to a capacitor **1310**, voltage feedback device **1112**, and a switch controller **1114***a*. Therefore, when input pad **1110** inputs a power supply, voltage feedback device **1112** takes a voltage signal between inductors **1320***a*, **1320***b*, **1320***c* and capacitor **1310** and sends a voltage feedback signal to switch controller **1114***a*. Switch controller **1114***a* then decides when MOS **1114***f*, **1114***g*, **1114***h*, **1114***i*, **1114***j*, **1114***k* will be switched on or off separately. The switch controller **1114***a* controls the duty cycles and on-off phases of switch MOS **1114***f*, **1114***g*, **1114***h*, **1114***i*, **1114***j*, **1114***k* to fine-tune the voltage level at output **1313**. When switch controller **1114***a* controls MOS **1114***f*, **1114***g*, **1114***h*, **1114***i*, **1114***j*, **1114***k*, at least two different on-off phases are generated. As shown in FIG. **20**, a result of output of FIG. **19**'s circuit when each switch MOS set with different switching phase, the voltage ripple of output is minimized by different on-off phases of switching MOS. Therefore, the present invention provides a semiconductor chip with a more stable power voltage.

Embodiment 7

FIG. **21***a* to FIG. **21***l* demonstrate a manufacturing process of a on-chip regulator or converter with inductor and capacitor, wherein the inductor is made by using post-passivation embossing process and the capacitor is attached by using surface mount technology.

Referring to FIG. **21***a*, integrated circuit **20** represents all structures below passivation layer **160**. Also included in integrated circuit **20** is substrate **100**, devices **110**, **112**, **114**, first dielectric layer **150**, metal layers **140**, second dielectric layer **155**, metal contact **120**, and metal via **130**, wherein multiple passivation layer openings **165***a* in passivation layer **160** reveal multiple pads **166***a*, **166***b*, and **166***c*.

Referring to FIG. **21***b*, an adhesion/barrier layer **401** is formed by sputtering on passivation layer **160** and contact pads **166***a*, **166***b*, and **166***c*. The thickness of said adhesion/barrier layer **401** is between 0.1 micrometers and 1 micrometer, with an optimal thickness between 0.3 micrometers and 0.8 micrometers. The material of adhesion/barrier **401** is preferred to be a TiW or Ti or Ti/TiW.

Referring to FIG. **21***c*, a seed layer **402** with a thickness between 0.05 micrometers and 1 micrometers (with an optimal thickness between 0.08 micrometers and 0.7 micrometers) is formed next on adhesion/barrier layer **401** by sputtering. In this embodiment, said seed layer **402** is made of gold preferentially. However, as described above, the material of seed layer **402** varies according to the material of metal layers formed afterwards.

Referring to FIG. **21***d*, photoresist layer **404** is formed on seed layer **402**, and through spin coating, exposure and development, photoresist layer **404** is patterned, forming multiple photoresist layer openings **404***a* in photoresist layer **404**, which separately reveal portions of seed layer **402** that are over pad **166***a*, **166***b*, and **166***c*.

Referring to FIG. **21***e*, bonding metal layer **406** is formed by an electroplating method on seed layer **402**, which is in photoresist layer opening **404***a*. The bonding metal layer **406** consists of materials such as gold, copper, silver, palladium, rhodium, ruthenium, rhenium, or nickel, and may have a single metal layer structure or multiple metal layer structure. The thickness of bonding metal layer **406** is between 1 micrometers and 100 micrometers, with optimal thickness between 1.5 micrometers and 15 micrometers. The combinations of the multiple metal layer structure comprise Cu/Ni/Au, Cu/Au, Cu/Ni/Pd, and Cu/Ni/Pt. In this embodiment, bonding metal layer **406** is preferred a single layer made of gold.

Referring to FIG. **21***f*, remove patterned photoresist layer **404** and portions of seed layer **402** and adhesive/barrier layer **401** that are not below metal layer **406**. Portions of seed layer **402** that are made of gold are removed by using solvents containing KI plus I_2 solution, while adhesive/barrier layer **401** is removed by using solvents containing hydrogen peroxide (H_2O_2) if the material of layer **401** is TiW.

Referring to FIG. **21***g*, after removing patterned photoresist layer **404** and portions of seed layer **402** and adhesive/barrier layer **401** that are not under metal layer **406**, said bonding metal layer **406** at least forms one inductor device **408**, multiple wire-bonding pads **410**, and multiple contact pads **412** on passivation layer **160**. Said wire-bonding pads **410** are formed on pad **166***a*, while said contact pads **412** are formed on pad **166***c*, and said inductor device **408** is formed on passivation layer **160** and pads **166***b*. FIG. **21***f* is a signified cross section view of FIG. **21***g* across horizontal line **2-2**. Multiple inductor devise **408** can also be formed on or over passivation layer **160**, as shown in FIG. **21***h*, but in this embodiment, only one inductor device **408** is demonstrated mainly.

Referring to FIG. **21***i*, a polymer layer **414** is formed on multiple wire-bonding pads **410**, multiple contact pads **412**, and passivation layer **160**.

Referring to FIG. **21***j*, through spin coating, exposure and development, etching and O2 plasma ash, polymer layer **414** is formed and patterned with multiple openings **414***a* that reveal multiple wire-bonding pads **410**, multiple contact pads, **412**, and cover inductor device **408**. Polymer layer **414** is then cured under a temperature between 150 and 380 degrees Celcius. The material of polymer layer **414** can be chosen from polyimide (PI), benzocyclobutene (BCB), parylene, epoxy-based material, such as epoxy resins or photoepoxy SU-8 provided by Sotec Microsystems of Swiss Renens, or elastomers, such as silicone. If polymer layer **414** is made of polyimide, it is preferred ester-type polyimide. The polymer layer **414** is preferred to be photosensitive, then lithography can be used to pattern said polymer layer **414**. Polymer layer **414** has a thickness between 5 micrometers and 50 micrometers, with an optimal thickness between 10 micrometers and 20 micrometers.

Referring to FIG. **21***k* and FIG. **21***l*, dicing procedures are used to cut substrate **100**, passivation layer **160**, and polymer layer **414** into multiple semiconductor chips **600**. Said multiple wire-bonding pads **410** on semiconductor chips **600** can be connected to external circuits or power sources through a wire **416** formed by a wire-bonding process. Contact pad **412** can then be connected to a capacitor device **418** with a solder layer **420**, through surface mount technique (SMT), wherein said capacitor device **418** is connected to inductor device **408** through metal layers **140** in integrated circuit **20**. Of course the dicing procedures can be performed after capacitor mounting.

Manufacturing Method and Structure 1 of Embodiment 8:

FIG. **22***a* to FIG. **22***m* demonstrate a manufacturing process of another on-chip regulator or converter with inductor and capacitor, wherein the inductor is made by using post-passivation embossing process and the capacitor is attached by using surface mount technology.

Referring to FIG. **22***a*, integrated circuit **20** represents all structures below passivation layer **160**. Also included in integrated circuit **20** is substrate **100**, devices **110**, **112**, **114**, first dielectric layer **150**, metal layers **140**, second dielectric layer **155**, metal contact **120**, and via **130**, wherein multiple passivation layer openings **165***a* in passivation layer **160** reveal multiple pads **166***a*, **166***b*, and **166***c*.

Referring to FIG. **22***b*, a polymer layer **421** is formed on passivation layer **160** and pads **166***a*, **166***b*, and **166***c*. Through spin coating, exposure and development, etching and O2 plasma ash, polymer layer **421** is formed and patterned with multiple openings **421***a* that reveal multiple pads **166***a*, **166***b*, and **166***c*. Polymer layer **421** is then cured under a temperature between 150 and 380 degrees Celcius. The material of polymer layer **421** can be chosen from polyimide (PI), benzocyclobutene (BCB), parylene, epoxy-based material, such as epoxy resins or photoepoxy SU-8 provided by Sotec Microsystems of Swiss Renens, or elastomers, such as silicone. If polymer layer **421** is made of polyimide, it is preferred ester-type polyimide. The polymer layer **421** is preferred to be photosensitive, then lithography can be used to pattern said polymer layer **421**. Polymer layer **421** has a thickness between 5 micrometers and 50 micrometers, with an optimal thickness between 10 micrometers and 25 micrometers.

Referring to FIG. **22***c*, an adhesion/barrier layer **422** is formed by sputtering on polymer layer **421** and pads **166***a*, **166***b*, and **166***c*. Said adhesion/barrier layer **422** has a thickness between 0.1 micrometers and 1 micrometer, with an optimal thickness between 0.3 micrometers and 0.8 micrometers. The material of adhesion/barrier **401** is preferred to be a TiW or Ti or Ti/TiW.

Referring to FIG. **22***d*, a seed layer **424** with a thickness between 0.05 micrometers and 1 micrometers (with an optimal thickness between 0.08 micrometers and 0.7 micrometers) is formed next on adhesion/barrier layer **422** by sputtering. In this embodiment, said seed layer **424** is made of gold preferentially. However, as described above, the material of seed layer **424** varies according to the material of metal layers formed afterwards.

Referring to FIG. **22***e*, photoresist layer **426** is formed on seed layer **424**, and through spin coating, exposure and development, photoresist layer **426** is patterned, forming multiple photoresist layer openings **426***a* in photoresist layer **426**, which separately reveal portions of seed layer **426** that are over pad **166***a*, **166***b*, and **166***c*.

Referring to FIG. **22***f*, bonding metal layer **428** is formed by an electroplating method on seed layer **424**, which is in photoresist layer opening **426***a*. The bonding metal layer **428** consists of materials such as gold, copper, silver, palladium, rhodium, ruthenium, rhenium, or nickel, and may have a single metal layer structure or multiple metal layer structure. The thickness of bonding metal layer **428** is between 1 micrometer and 100 micrometers, with optimal thickness between 1.5 micrometers and 15 micrometers. Layer **428** may be combinations of multiple metal layer structure comprising Cu/Ni/Au, Cu/Au, Cu/Ni/Pd, and Cu/Ni/Pt. In this embodiment, bonding metal layer **428** is a single layer made of gold preferentially.

Referring to FIG. **22***g*, remove patterned photoresist layer **426** and portions of seed layer **424** and adhesive/barrier layer **422** that are not below metal layer **428**. Seed layer **424** that are made of gold are removed by using solvents containing KI plus I_2 solution, while adhesive/barrier layer **422** is removed by using solvents containing hydrogen peroxide (H_2O_2) if the material of layer **422** is TiW.

Referring to FIG. **22***h*, after removing patterned photoresist layer **426** and portions of seed layer **424** and adhesive/barrier layer **422** that are not under metal layer **428**, said bonding metal layer **428** at least forms one inductor device **430**, multiple wire-bonding pads **432**, and multiple contact pads **434** on polymer layer **421**. Said wire-bonding pads **432** are formed on pad **166***a*, while said contact pads **434** are formed on pad **166***c*, and said inductor device **430** is formed on or over passivation layer **160** and pads **166***b*. FIG. **21***f* is a signified cross section view of FIG. **21***g* cut across horizontal line **2-2**. Multiple inductor devices **430** can also be formed on polymer **421**, as shown in FIG. **22***i*, but in this embodiment, only one inductor device **408** is demonstrated mainly.

Referring to FIG. **22***j*, a polymer layer **436** is formed by using spin coating on inductor device **430**, multiple wire-bonding pads **432**, multiple contact pads **434**, and polymer layer **421**.

Referring to FIG. **22***k*, through exposure and development, etching, and O2 plasma ash polymer layer **436** form multiple openings **436***a* that reveal multiple wire-bonding pads **432**, multiple contact pads **434**, and conceal inductor device **430**. Polymer layer **436** is then cured under a temperature between 150 and 380 degrees Celcius. The material of polymer layer **436** can be chosen from polyimide (PI), benzocyclobutene (BCB), parylene, or ester type polymers, such as epoxy resins or photoepoxy SU-8 provided by Sotec Microsystems of Swiss Renens, or elastomers, such as silicone. If polymer layer **436** is made of polyimide, it is preferred ester-type polyimide. The polymer layer **436** is photosensitive preferentially, then lithography can be used to pattern said polymer layer **436**. Polymer layer **436** has a thickness between 5 micrometers and 50 micrometers, with an optimal thickness between 10 micrometers and 20 micrometers.

Referring to FIG. **22***l* and FIG. **22***m*, dicing procedures are used to cut substrate **100**, passivation layer **160**, polymer layer **421**, and polymer layer **436** into multiple semiconductor chips **600**. Said multiple wire-bonding pads **432** on semiconductor chips **600** can be connected to external circuits or power sources through a wire **416** formed by a wire-bonding process. Contact pad **434** can then be connected to a capacitor device **418** with a solder layer **420**, through surface mount technique (SMT), wherein said capacitor device **418** is connected to inductor device **430** through metal layers **140** in integrated circuit **20**. Of course the dicing procedures may be performed after capacitor mounting.

Manufacturing method and structure 2 of Embodiment 8:

Continuing from FIG. **22***k* and referring to also FIG. **22***n* and FIG. **22***o*, the inductor **430** and the pads **166***b* are between the contact pads **434** and the pads **166***c*.

Referring to FIG. **22***p* and FIG. **22***q*, dicing procedures are used to cut substrate **100**, passivation layer **160**, polymer layer **421**, and polymer layer **436** into multiple semiconductor chips **600**. Said multiple wire-bonding pads **432** on semiconductor chips **600** can be connected to external circuits or power sources through a wire **416** formed by a wire-bonding process. Contact pad **434** can then be connected to a capacitor device **418** with a solder layer **420**, through surface mount technique (SMT), wherein said capacitor device **418** is connected to inductor device **430** through metal layer **428** or metal layers **140** in integrated circuit **20**. Of course the dicing procedures may be performed after capacitor mounting.

Embodiment 9

Referring to FIG. **23***a* and FIG. **23***b*, this embodiment is similar to Embodiment 8, with the only difference being the location of wire-bonding pad **432** and pad **166***a*. In Embodiment 8, wire-bonding bad **432** is directly above pad **166***a*, but in this embodiment, wire-bonding pad **432** is not directly above pad **166***a*. Therefore, the location of wire-bonding pad **432** can be adjusted according to requirement and not limited to the area directly above pad **166***a*.

Embodiment 10

Referring to FIG. **24***a* and FIG. **24***b*, this embodiment is similar to Embodiment 8, with the difference being a connecting point **438** of inductor devices revealed by multiple openings **436***a* in polymer layer **436**. Connecting point **438** can be connected to external circuits or power sources using a wire **416** made by a wire-bonding process.

Embodiment 11

Referring to FIG. **25***a*, integrated circuit **20** represents all structures below passivation layer **160**. Also included in integrated circuit **20** is substrate **100**, devices **110**, **112**, **114**, first dielectric layer **150**, metal layers **140**, second dielectric layer **155**, metal contact **120**, and metal via **130**, wherein multiple passivation layer openings **165***a* in passivation layer **160** reveal multiple pads **166***a*, **166***b*, and **166***c* (Pad **166***a* is not labeled in FIG. **25***a*, but is in FIG. **25***b*).

Referring to FIG. **25***b*, an adhesion/barrier layer **401** is formed by sputtering on passivation layer **160** and contact pads **166***a*, **166***b*, and **166***c*. The thickness of said adhesion/barrier layer **401** is between 0.1 micrometers and 1 micrometer, with an optimal thickness between 0.3 micrometers and 0.8 micrometers. The material of adhesion/barrier **401** is preferred to be a TiW or Ti or Ti/TiW.

Referring to FIG. **25***c*, a seed layer **402** with a thickness between 0.05 micrometers and 1 micrometers (with an optimal thickness between 0.08 micrometers and 0.7 micrometers) is formed next on adhesion/barrier layer **401** by sputtering. In this embodiment, said seed layer **402** is made of gold preferentially. However, as described above, the material of seed layer **402** varies according to the material of metal layers formed afterwards.

Referring to FIG. **25***d*, photoresist layer **404** is formed on seed layer **402**, through spin coating, exposure and development, photoresist layer **404** is patterned, forming multiple photoresist layer openings **404***a* in photoresist layer **404**, which separately reveal portions of seed layer **402** that are over pad **166***a*, **166***b*, and **166***c*.

Referring to FIG. **25***e*, bonding metal layer **406** is formed by an electroplating method on seed layer **402**, which is in photoresist layer opening **404***a*. The bonding metal layer **406** consists of materials such as gold, copper, silver, palladium, rhodium, ruthenium, rhenium, or nickel, and may have a single metal layer structure or multiple metal layer structure. The thickness of bonding metal layer **406** is between 1 micrometer and 100 micrometers, with optimal thickness between 1.5 micrometers and 15 micrometers. Layer **406** may be combinations of multiple metal layer structure comprising Cu/Ni/Au, Cu/Au, Cu/Ni/Pd, and Cu/Ni/Pt. In this embodiment, bonding metal layer **406** is preferred to be a single layer made of gold.

Referring to FIG. **25***f*, remove patterned photoresist layer **404** and portions of seed layer **402** and adhesive/barrier layer **401** that are not below metal layer **406**. Seed layer **402** that are made of gold are removed by using solvents containing I_2, while adhesive/barrier layer **401** is removed by using solvents containing hydrogen peroxide (H_2O_2) if the material of layer **401** is TiW. After removing patterned photoresist layer **404** and portions of seed layer **402** and adhesion/barrier layer **401** that is not under bonding metal layer **406**, said bonding metal layer **406** includes multiple wire-bonding pads **440** and multiple contact pads **442**, wherein a wire-bonding pad **440** and a contact pad **442** are connected through bonding metal layer **406**.

Referring to FIG. **25***g*, a polymer layer **414** is formed by using spin coating on multiple wire-bonding pads **440**, multiple contact pads **442**, and passivation layer **160**.

Referring to FIG. **25***h*, through exposure and development, and O2 plasma ash, polymer layer **444** is patterned with multiple openings **444***a* that reveal multiple wire-bonding pads **440** and multiple contact pads **442**. Polymer layer **444** is then cured under a temperature between 150 and 380 degrees Celcius. The material of polymer layer **444** can be chosen from polyimide (PI), benzocyclobutene (BCB), parylene, epoxy-based material, such as epoxy resins or photoepoxy SU-8 provided by Sotec Microsystems of Swiss Renens, or elastomers, such as silicone. If polymer layer **444** is made of polyimide, it is preferred ester-type polyimide. The polymer layer **444** is photosensitive preferentially, then lithography can be used to pattern said polymer layer **444**, and the etching process will be unnecessary. Polymer layer **444** has a thickness between 5 micrometers and 50 micrometers, with an optimal thickness between 10 micrometers and 25 micrometers.

Referring to FIG. **25***i* and FIG. **25***j*, dicing procedures are used to cut substrate **100**, passivation layer **160**, and polymer layer **444** into multiple semiconductor chips **600**. Said multiple wire-bonding pads **440** on semiconductor chips **600** can be connected to external circuits or power sources through a wire **416** formed by a wire-bonding process. Contact pad **442** can then be connected to a capacitor device **448** with a solder layer **420**, through surface mount technique (SMT), wherein said capacitor device **448** is connected to inductor device **448** through metal layers **140** in integrated circuit **20**. FIG. **25***j* is a cross section view of FIG. **25***k* from horizontal line **2**-**2**. Of course the dicing procedures may be performed after capacitor mounting.

Embodiment 10 and Embodiment 11 can be used in devices that step-up voltage as shown in circuit diagrams of FIG. **26** and FIG. **27**. In FIG. **26**, power source input **2240** is connected to inductor **2320**, inductor **2320** is connected to capacitor **2310** through transistor **2114***d*, voltage feedback device **2112** is connected to power output **2110**, and switch controller **2114***a* is connected to voltage feedback device **2112** and a switch transistor **2114***b*. When power enters through power input **2240**, switch controller **2114***a* receives the voltage signal of voltage feedback device **2112** and controls the on and off timing of switch transistor **2114***b*, pumping up the voltage level of power source output **2110**. Inductor **2320** together with capacitor **2310**, voltage feedback device **2112**, switch transistor **2114***b* and transistor **2114***d* form an on-chip voltage regulator or converter with the previous described manufacture processes.

The difference between FIG. **27** and FIG. **26** is that the circuit diagram of FIG. **27** is made of multiple inductors **2320**, capacitor **2310**, switch transistor **2114***g*, switch transistor **2114***i*, transistor **2114***h* and transistor **2114***f*. Switch controller **2114***a* is used to receive the voltage signal of voltage feedback device **2112** and control the duty cycle and phase of switch transistor **2114***g*, and switch transistor **2114***i* and therefore pumping up the voltage level of power output **2110**. In comparison to the circuit diagram of FIG. **26**, the circuit diagram of FIG. **27** can be more accurately and efficiently to regulate the output voltage.

From the description above, it can be known that the present invention discloses a semiconductor chip and its application circuit, wherein in the passive and active devices are integrated with the semiconductor chip, so that the signal path between the two types of devices has minimal distance, therefore enabling fast and effective voltage regulation and also decreasing circuit routing area on the PCB. Most importantly, the reaction time of each device is decreased, increasing the performance of electronic device without increasing cost.

While this invention has been described in terms of the above specific embodiment(s), those skilled in the art will recognize that the invention can be practiced with modifications within the spirit and scope of the appended claims, i.e. that changes can be made in form and detail, without departing from the spirit and scope of the invention. Accordingly all such changes come within the purview of the present invention and the invention encompasses the subject matter of the claims which follow.

What is claimed is:

1. A semiconductor chip comprising:

a semiconductor substrate;

multiple active devices in said semiconductor substrate;

a first dielectric layer coupled to said semiconductor substrate;

a conductive structure coupled to said first dielectric layer and said semiconductor substrate, wherein said conductive structure comprises a first conductive layer and a second conductive layer coupled to said first conductive layer, wherein said first conductive layer and said second conductive layer comprise an inductor within the semiconductor chip;

a second dielectric layer between said first and second conductive layers;

a passivation layer coupled to said first and second conductive layers and said first and second dielectric layers, wherein said passivation layer comprises a nitride;

a discrete capacitor coupled to said passivation layer; and

a solder between said discrete capacitor and a contact point of said conductive structure.

2. The semiconductor chip of claim **1**, wherein said first conductive layer comprises a copper layer having a thickness between 0.05 and 2 micrometers.

3. The semiconductor chip of claim **1**, wherein said nitride has a thickness between 0.3 and 2 micrometers.

4. The semiconductor chip of claim **1**, wherein said conductive structure comprises a gold-containing layer coupled to said solder.

5. The semiconductor chip of claim **1**, wherein said conductive structure comprises a nickel layer coupled to said solder.

6. The semiconductor chip of claim **1**, wherein said conductive structure comprises a copper layer coupled to said solder.

7. The semiconductor chip of claim **1**, further comprising a polymer layer coupled to said passivation layer, wherein said inductor and said discrete capacitor are coupled to said polymer layer.

8. The semiconductor chip of claim **1**, further comprising a polymer layer coupled to said inductor and said passivation layer, wherein said discrete capacitor is further coupled to said polymer layer.

9. The semiconductor chip of claim **1**, wherein said conductive structure has a region configured to be wirebonded thereto.

10. The semiconductor chip of claim **1**, wherein said inductor is coupled to said passivation layer.

11. A circuit component comprising:

a semiconductor substrate;

multiple active devices in said semiconductor substrate;

a first dielectric layer coupled to said semiconductor substrate;

a conductive structure coupled to said first dielectric layer, wherein said conductive structure comprises a first conductive layer and a second conductive layer coupled to said first conductive layer, wherein said first conductive layer and said second conductive layer comprise an inductor within said circuit component;

a second dielectric layer between said first and second conductive layers;

a passivation layer coupled to said first and second conductive layers and said first and second dielectric layers, wherein said passivation layer comprises a nitride;

a discrete capacitor coupled to said passivation layer; and

a solder coupled to said discrete capacitor.

12. The circuit component of claim **11**, wherein said first conductive layer comprises a copper layer having a thickness between 0.05 and 2 micrometers.

13. The circuit component of claim **11**, wherein said nitride has a thickness between 0.3 and 2 micrometers.

14. The circuit component of claim **11**, wherein said conductive structure comprises a gold-containing layer coupled to said solder.

15. The circuit component of claim **11**, wherein said conductive structure comprises a nickel layer coupled to said solder.

16. The circuit component of claim **11**, wherein said conductive structure comprises a copper layer coupled to said solder.

17. The circuit component of claim **11**, further comprising a polymer layer coupled to said passivation layer, wherein said inductor and said discrete capacitor are coupled to said polymer layer.

18. The circuit component of claim **11**, further comprising a polymer layer coupled to said inductor and said passivation layer, wherein said discrete capacitor is further coupled to said polymer layer.

19. The circuit component of claim **11**, wherein said second conductive layer comprises aluminum.

20. The circuit component of claim **11**, wherein said inductor is coupled to said passivation layer.

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