Supply-Noise Resilient Adaptive Clocking for Battery-Powered Aerial Microrobotic System-on-Chip in 40nm CMOS

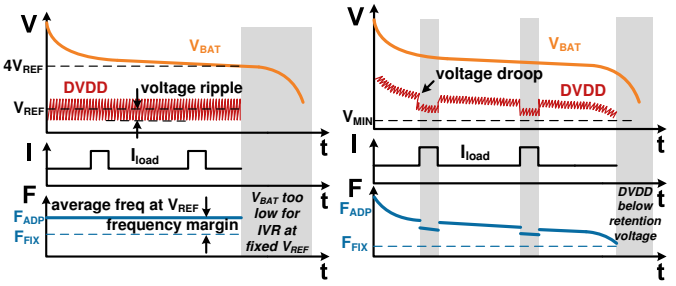
Xuan Zhang, Tao Tong, David Brooks, Gu-Yeon Wei
Harvard University, Cambridge, MA 02138
Email: xuanzhang@eecs.harvard.edu

***Abstract*—A battery-powered aerial microrobotic System-on-Chip (SoC) has stringent weight and power budgets, which requires fully-integrated solutions for both clock generation and voltage regulation. Supply-noise resilience is important yet challenging for such SoC systems due to a non-constant battery discharge profile and load current variability. This paper proposes an adaptive-frequency clocking scheme that can tolerate supply noise and improve performance when implemented with an integrated voltage regulator (IVR). Measurements from a 'brain' SoC, implemented in 40nm CMOS, demonstrate $2\times$ performance improvement with adaptive-frequency clocking over conventional fixed-frequency clocking. Combining adaptive-frequency clocking with open-loop IVR extends error-free operation to a wider battery voltage range (2.8 to 3.8V) with higher average performance.**

I. Introduction

System-on-chip (SoC) for aerial microrobots faces stringent weight and size constraints; at the same time, it requires considerable performance and power to handle a variety of tasks such as image sensing, navigation, and flight control. Conventional digital systems typically operate at a fixed frequency with respect to an external clock source and off of a constant voltage supplied by an external voltage regulator. However, in order to demonstrate an autonomous flying robotic insect with limited lift force generated by its wings [6], a 'brain' SoC designed for the Harvard RoboBee must be powered directly off of a battery with no external components. In order to meet this stringent constraint, the SoC system employs an integrated voltage regulator (IVR) and an internal voltage-tracking clock generator for its digital logic and memories.

One of the main objectives of this work is to maximize the RoboBee's flight time with respect to the total energy available in its battery and the associated battery discharge profile. In this vein, this paper explores the relative merits of different operational modes offered by the IVR and on-chip clock generator. The IVR is a 4:1 switched-capacitor (SC) converter that cascades two 2:1 SC stages individually tuned to maximize conversion efficiency [7]. This SC-IVR converts the 3.6-4V battery voltage down to 0.9V and below for the digital SoC load. It can operate in either open- or closed-loop regulation modes. Fig. 1 illustrates these two possible modes of operation with respect to a discharge profile, typical of lithium-based batteries. In closed-loop operation (regulated voltage), the SC-IVR works to provide a constant supply voltage that is resilient to input battery (V_{BAT}) and output load (I_{LOAD}) conditions. However, for a target output voltage level (V_{REF}), the SC-IVR's operating range is limited to $V_{\text{BAT}} > 4V_{\text{REF}}$. In contrast, open-loop operation (unregulated voltage) exhibits an entirely different set of attributes; the SC-IVR's output voltage is roughly 1/4th the input battery voltage, but varies



(a) closed-loop regulation (b) open-loop operation

Fig. 1: Illustrations of two SC-IVR modes of operation versus typical battery dicharge profile.

with both the discharge profile and load fluctuations. While open-loop SC-IVR mode allows the system to operate over a wider range, down to the minimum voltage limit of the digital load, performance and efficiency of energy utilization depends on the clocking strategy used. Hence, we also explore two clocking schemes: *fixed-frequency* and *adaptive-frequency* clocking. Out of the four total combinations, this paper compares the following three: (1) regulated voltage, fixed frequency; (2) regulated voltage, adaptive frequency; and (3) unregulated voltage, adaptive frequency. With closed-loop voltage regulation, fixed-frequency clocking (F_{FIX}) requires extra timing margins to account for non-negligible voltage ripple, which is an artifact of the SC-IVR's feedback loop. Alternatively, an adaptive-frequency clocking (F_{ADP}) scheme offers higher average frequency . Adaptive-frequency clocking also works well for open-loop SC-IVR mode, because it maximizes performance with respect to battery and load conditions.

In order to explore the relative tradeoffs and merits associated with the different operational modes described above, the remainder of the paper first describes the SC-IVR and clock generator designed into the prototype 'brain' SoC implemented in TSMC's 40nm process. Then, Section III presents experimental results that verify the performance advantages of using adaptive clocking with both regulated and unregulated voltages generated by the SC-IVR.

II. System Architecture

The brain SoC designed for the RoboBee, shown in Fig. 2, contains a fully-integrated two-stage 4:1 switched-capacitor voltage regulator (SC-IVR), a 32-bit ARM Cortex-M0 general-purpose processor, two identical 64KB memories, and a programmable digitally-controlled oscillator (DCO) that generates the voltage-tracking adaptive-frequency clock. The test chip also includes numerous blocks for test and debug purposes: a built-in self test (BIST) block allows thorough testing of the two memory blocks; a scan chain configures the digital blocks;

978-1-4673-6146-0/13/$31.00 ©2013 IEEE

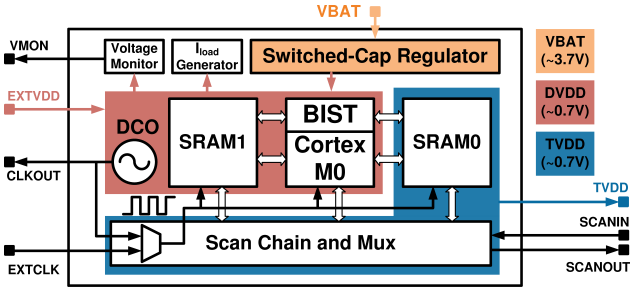


Fig. 2: Block diagram of the fully-integrated SoC.

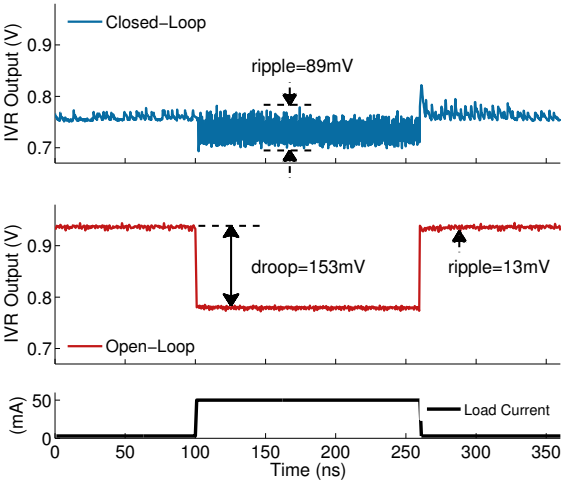


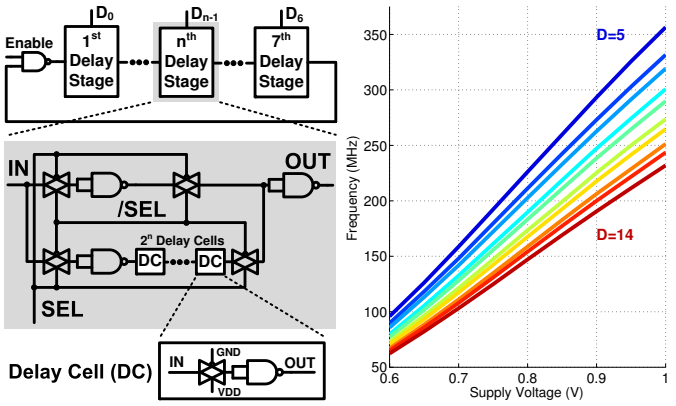
Fig. 3: Transient response of SC-IVR output voltage to load current steps.

a voltage monitor block probes internal supply voltages; and a current-load generator enables different IVR testing scenarios. Lastly, the test chip allows for external power and clock sources to investigate different operating modes.

A. *Switched-capacitor integrated voltage regulator*

The SC-IVR converts the battery voltage ($V_{\text{BAT}} \approx 3.7V$) down to the digital supply (DVDD $\approx 0.7V$). It consists of a cascade of two 2:1 switched-capacitor converters that are respectively optimized for high input voltage tolerance and fast load response, and each converter stage employs a 16-phase topology to reduce voltage ripple. A low-boundary feeback control loop can regulate DVDD to a desired voltage level. A thorough discussions of the SC-IVR and its implementation details can be found in [7].

While this SC-IVR achieves high conversion efficiency, 70% at its optimal operating point, it is subject to the inherent limitations of any switched-capacitor based DC-DC converter; efficiency varies with respect to input and output voltages and the load. Extensive measurement results in [7] show that open-loop operation consistently offers higher conversion efficiency. Fig. 3 plots transient behavior of the IVR with respect to load current steps between 3mA and 50mA for both open- and closed-loop operation. Closed-loop operation quickly responds to avoid the steep voltage droop otherwise seen in the open-loop case; however, it exhibits larger steady-state voltage ripple, especially for higher load currents, due to the control loop topology and feedback delay.



(a) DCO schematic

(b) DCO frequency versus DVDD at digital control code D

Fig. 4: Digital-controlled oscillator schematic and measured characteristics.

B. *Digitally-controlled oscillator*

Our proposed adaptive-frequency clocking scheme needs a clock generator whose frequency tracks closely with changes in supply voltage. This allows the operating frequency of the digital load circuitry to appropriately scale with voltage fluctuations, providing intrinsic resilience to supply noise. There are numerous examples of critical-path-tracking circuits for local timing generation [3], [2]. Instead, we use a programmable digitally-controlled oscillator (DCO) to generate the system clock. The DCO contains a ring of programmable delay cells comprising transmission and NAND gates that approximate a typical fanout-of-4 inverter delay. Such designs have been found to deliver decent tracking accuracy, acting as a proxy for critical path delay in complex digital logic [1], [4], [8].

As shown in Fig. 4(a), a digital code, $D = D_7...D_1D_0$, sets the DCO frequency by selecting the number of delay cells in the oscillator loop. While our implementation uses 7 bits of control code, measurement results show that the lower 4 bits are sufficient for the normal operating range of the digital load. Fig. 4(b) plots DCO frequency versus supply voltage (DVDD) across a range of the digital control codes. Across the measured voltage range (0.6 to 1V), frequency scales roughly linearly with voltage, but slightly flattens out for voltages below 750mV. The uneven frequency spacing with respect to D results from the delay cell's asymmetric design.

C. *Cortex-M0 and memory*

The Cortex-M0 microprocessor and one of the 64KB memories (SRAM1) share the voltage domain (DVDD) with the DCO. A built-in self-test (BIST) module performs at-speed test of the SRAMs. To make sure all of the memory cells are thoroughly tested, the BIST performs a modified MARCH-C routine that writes and reads different data patterns to and from every address in the SRAMs. The BIST module raises a pass/fail flag at the conclusion of the MARCH-C routine, and the address and data of the last failure are recorded for post-test analysis.

SRAM0 shares the same physical design as SRAM1, but operates off of a separate voltage domain (TVDD) along with other test peripherals such as a voltage monitor circuit that captures fast nanosecond-scale supply transients. The SoC is

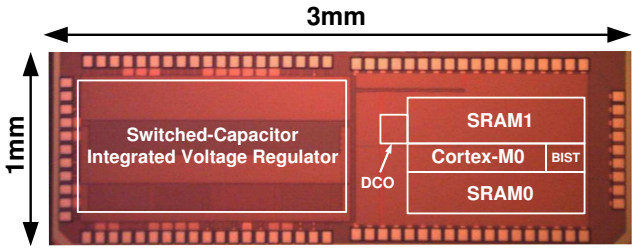


Fig. 5: Die photo of the fully-integrated system-on-chip

capable of operating directly off of the battery without any external supply or clock reference. TVDD, EXTVDD, and EXTCLK were added for testing purposes only.

III. Experimental Results

To demonstrate improved resilience and performance of the proposed adaptive clocking across a wide range of supply voltage, measurement results were obtained from a prototype SoC chip (Fig. 5) fabricated in TSMC's 40nm CMOS technology. We use the maximum error-free operating frequency of the memory performing built-in self-test as a proxy metric, because it is often the on-chip SRAM sharing the same voltage domain with the digital logic that limits the system performance at lower supply levels. Also, the retention voltage of the SRAM cells typically determines the minimum operating voltage of the system [5].

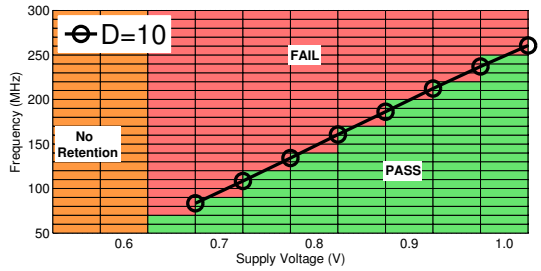
This section presents the following set of experimental results: First, we characterize the voltage versus frequency relationship of the SRAMs using external sources in order to determine the efficacy of using the DCO for adaptive-frequency clocking. Then, we compare the fixed- and variable-frequency clocking schemes with a regulated voltage generated by the SC-IVR in closed-loop operation. Lastly, we present the advantages of combining adaptive clocking with a variable voltage provided by operating the SC-IVR in open loop.

A. Frequency vs. voltage characterization

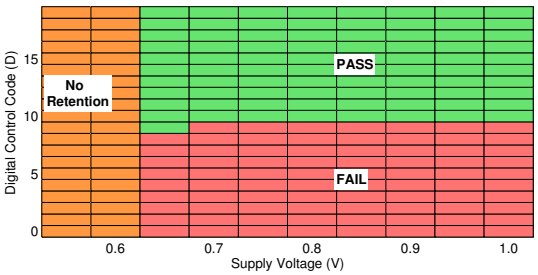
The on-chip SRAMs were characterized at static supply voltage levels provided externally via EXTVDD, in order to determine the SRAM's voltage to frequency relationship under quiet supply conditions. Using an external clock (EXTCLK) at different fixed frequencies, we obtained the Shmoo plot in Fig. 6(a). It shows (1) the minimum retention voltage of SRAM cell is between 0.6V and 0.65V; (2) the maximum SRAM frequency scales roughly linear with supply voltage and ranges from 68MHz at 0.65V to 256MHz at 1.0V; and (3) the maximum SRAM frequency closely correlates with DCO frequency plot for control code D=10. This correlation suggests the FO4-delay-based DCO tracks the critical path delay in the SRAM across a wide supply range and should enable error-free memory BIST for control word D above 10. We experimentally verified this by turning on the internal DCO to provide the system clock instead of using EXCLK and sweeping the same voltage range via EXTVDD. The resulting Shmoo plot in Fig. 6(b) further demonstrates the DCO's ability to track SRAM delay at different static supply voltage levels.

B. Fixed vs. adaptive clocking with regulated voltage

Having verified the DCO, we now compare fixed- and adaptive-frequency clocking schemes for a system that operates off of a regulated voltage with the SC-IVR operating in closed loop. We also emulate noisy operating conditions using the on-chip I_{LOAD} generator that switches between 0 and 15mA at 1MHz. Measurements made via the on-die voltage monitoring circuit showed approximately $\pm 70mV$ worst-case ripple about a mean voltage of 0.714V.



(a) External clock at fixed frequencies



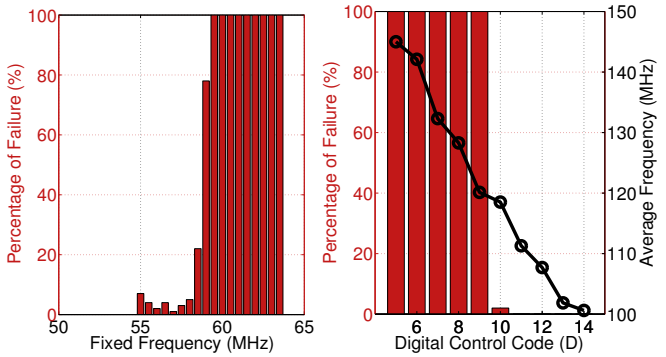
(b) Internal adaptive clock generated by the DCO at different control code (D)

Fig. 6: Shmoo plots for two different clocking schemes

For the conventional fixed-freqeuency clocking scheme, the maximum operating frequency ought to depend on the worst-case voltage droop, measured to be 0.647V. Using the measured relationship in Fig. 6(a), the maximum frequency cannot exceed 68MHz. To measure the actual maximum error-free frequency, we performed 100 independent BIST runs using the external clock, EXTCLK, set to a fixed frequency and recorded the failure rate. Fig. 7(a) summarizes the measured failure rates across different externally driven operating frequencies. These results show that the maximum error-free frequency is below 55MHz for the fixed-frequency clocking scheme, which is even lower than the anticipated 68MHz, perhaps attributable to the additional noise injection.

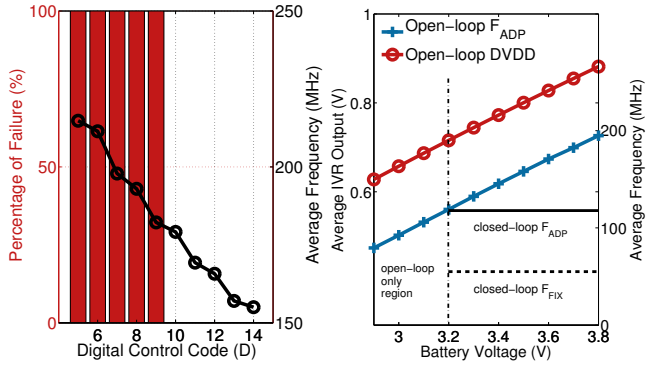
Using the same IVR configuration and test conditions, Fig. 7(b) plots the failure rates versus different digital control codes of the DCO. At D=10, there were intermittent failures, attributable to the additional noise not present in the prior experiemental results of Fig. 6(b). The adaptive-frequency clocking scheme delivers consistent and reliable operation at D=11. Based on the average DCO frequency measured during the tests and also plotted in Fig. 7(b), D=11 corresponds to an average frequency of 111MHz, which is 2× the fixed-frequency clocking scenario.

We can attribute this large frequency difference between the two clocking scenarios to a couple of factors. Fixed-frequency clocking requires sufficiently large guardbands to guarantee operation under the worst-possible voltage droop condition. In contrast, adaptive-frequency clocking allows both the clock period and load circuit delays to fluctuate together as long as both vary with voltage in a similar manner. Hence,



(a) Fixed-frequency externally (b) Adaptive-frequency from DCO

Fig. 7: Comparison of memory BIST failure rates for fixed- vs. adaptive-frequency clocks, but under the same IVR closed-loop regulation.



(a) Failure rate and average frequency vs. DCO settings (b) Measured average clock frequency and output voltage

Fig. 8: Performance under unregulated voltage from open-loop SC-IVR operation.

the guardband must only cover voltage-tracking deviations between the DCO and load circuit delay paths across the operating voltage range of interest, and can be built into the DCO. Another factor that penalizes the performance of the fixed-frequency clocking comes from the additional noise on the external clock signal for crossing the TVDD to DVDD boundary.

C. Adaptive-frequency clocking with unregulated voltage

We now turn our attention to how adaptive-frequency clocking performs with an unregulated voltage generated by the SC-IVR operating in open loop. We used the same test setup with $V_{BAT} = 3.7V$ and noise injection via the on-chip I_{LOAD} generator. The failure rates and the average frequencies are captured in Fig. 8. Compared to the measured results in Fig. 7(b), average frequencies are much higher, because DVDD settles to higher values ($\approx 0.8V$) when the SC-IVR operates in open loop. Despite the high susceptibility to fluctuations on DVDD to load current steps as seen in Fig. 3, Fig. 8(a) shows zero errors occured even for D=10. The higher DVDD voltage provides more cushion to avoid intermittent retention failure.

In order to illustrate the extended operating range offered by running the SC-IVR in open loop, Fig. 8(b) plots the average DCO frequency and average DVDD voltage for error-free operation versus battery voltage. These measurements were again made with 0 to 15mA current load steps. As expected, the open-loop SC-IVR's average output voltage scales proportional to the battery voltage. Moreover, the system can operate error-free even for battery voltages below 3V, which approaches the 2.5-2.7V lower discharge limit of Li-ion batteries. In comparison, assuming a target SC-IVR regulated voltage of 0.7V, the system would only operate down to a battery voltage of 3.2V and at a lower frequency across the battery discharge profile even with the adaptive-frequency clocking scheme. A fixed-frequency clocking scheme would lead to even lower performance.

In addition to validating the resilience and the performance advantages of adaptive-frequency clocking, our experimental results also reveal the synergistic properites between the clocking scheme and the IVR design in a battery-powered SoC system. The supply-noise resilience provided by an adaptive clock alleviates design constraints imposed by voltage ripple and voltage droop. Therefore, the IVR can trade off its transient response for better efficiency or smaller area when co-designed with adaptive-frequency clocking.

IV. Conclusion

An adaptive-frequency clocking scheme offers several advantages when combined with an IVR in an SoC, fabricated in 40nm CMOS, for battery-powered aerial microrobotic applications. For regulated voltage operation via closed-loop SC-IVR, adaptive-frequency clocking enables $2\times$ performance improvement, compared to conventional fixed-frequency clocking. Combining adaptive-frequency clocking with an unregulated voltage via open-loop IVR extends the operating range across a wider portion of the battery discharge profile. Finally, the noise resilience demonstrated by the adaptive-frequency clocking scheme calls for co-design and co-optimization of clock generation and voltage regulation in weight-and-power constraint integrated systems.

Acknowledgment

The authors thank the TSMC university shuttle program for chip fabrication. This work was supported in part by the National Science Foundation (NSF) Expeditions in Computing Award #: CCF-0926148.

References

[1] T. D. Burd et al. A dynamic voltage scaled microprocessor system. *JSSC*, 35(11), 2000.

[2] I. J. Chang et al. Exploring asynchronous design techniques for process-tolerant and energy-efficient subthreshold operation. *JSSC*, 45(2), 2010.

[3] M. E. Dean. *STRiP: a self-timed RISC processor*. PhD thesis, Stanford University, 1992.

[4] Y. Ikenaga et al. A 27% active-power-reduced 40-nm CMOS multimedia SoC with adaptive voltage scaling using distributed universal delay lines. *JSSC*, 47(4), 2012.

[5] S. Jain et al. A 280mV-to-1.2V wide-operating-range IA-32 processor in 32nm CMOS. In *ISSCC*, 2012.

[6] M. Karpelson et al. Energetics of flapping-wing robotic insects: Towards autonomous hovering flight. In *IROS*, 2010.

[7] T. Tong et al. A fully integrated battery-connected switched-capacitor 4:1 voltage regulator with 70% peak efficiency using bottom-plate charge recycling. Submitted to CICC, 2013.

[8] G.-Y. Wei and M. Horowitz. A fully digital, energy-efficient, adaptive power-supply regulator. *JSSC*, 34(4), 1999.