A Low Mass Power Electronics Unit to Drive Piezoelectric Actuators for Flying Microrobots

Mario Lok, Elizabeth Farrell Helbling, Xuan Zhang, *Member, IEEE*, Robert Wood, David Brooks, and Gu-Yeon Wei

***Abstract*—This paper presents a power electronics design for the piezoelectric actuators of an insect-scale flapping-wing robot, the RoboBee. The proposed design outputs four high-voltage drive signals tailored for the two bimorph actuators of the RoboBee in an alternating drive configuration. It utilizes fully integrated drive stage circuits with a novel highside gate driver to save chip area and meet the strict mass constraint of the RoboBee. Compared with previous integrated designs, it also boosts efficiency in delivering energy to the actuators and recovering unused energy by applying three power saving techniques, dynamic common mode adjustment, envelope tracking, and charge sharing. Using this design to energize four 15 nF capacitor loads with a 200 V and 100 Hz drive signal and tracking the control commands recorded from an actual flight experiment for the robot, we measure an average power consumption of 290 mW.**

***Index Terms*—BCD, capacitive loads, high voltage driver, microrobot, piezoelectric (PZT) actuator driver.**

I. Introduction

HARVARD's RoboBee is a centimeter-scale biologically inspired microair vehicle with promising potential in applications such as exploration, environment monitoring, and surveillance. Lift is produced by two bimorph piezoelectric (PZT) actuators that drive flapping-wing locomotion [1]. Recent demonstrations of hovering and maneuvering along three axes marked an important milestone in the project [1]. However, this demonstration uses a bench-top high-voltage amplifier to energize PZT actuators that flap its wings. To achieve full autonomy, one requirement is that the robot must carry the power electronics unit (PEU) that drives the actuator. This paper presents the latest integrated design for a PEU that drives the actuators of the RoboBee with a total component weight of 70 mg.

The PZT actuator on the RoboBee was selected for its high power density at actuation frequencies on the order of 100 Hz and manufacturability at small scales [2], [3]. However, the high-voltage drive requirement, the capacitive nature of the actuators, and the stringent weight budget present opposing challenges to the design of onboard power electronics [4].

As shown in [1], the actuators require a 200 V sinusoidal excitation voltage at around 100 Hz. However, a typical energy source compatible with the weight budget for full autonomy has an output voltage of 3.7 V. Consequently, the PEU needs to support a large step-up ratio. Since the two bimorph PZT actuators present a total of four capacitive loads, the driver circuitry must provide multiple output channels. Moreover, each of these output channels should support efficient bidirectional energy flow, such that they can both deliver energy to the actuator and recover unused energy stored in the capacitive structure of the actuator. Finally, the RoboBee has a payload weight budget of 170 mg [5], shared by the sensors, power electronics, a microcomputer, and a battery. For the PEU, the low mass requirement limits the size and number of energy storage elements such as inductors and capacitors that can be used in the design. This further increases the difficulty in achieving efficient energy conversion from low voltage to high voltage and efficient bidirectional energy flow for multiple capacitive loads.

Prior works have shown several topologies suitable for generating the high output voltage needed when using a battery to drive PZT actuators. These topologies include flyback converters [6], tapped-inductor boost converters [6], [7], and quadratic converters [8]. In addition, other actuator drivers have demonstrated single-stage converters that enable efficient energy delivery to and recovery from capacitive loads [9].

In contrast to single-stage converters, previous work targeting the RoboBee power electronics relied on a dual-stage power electronics design [4]. In the first stage, a tap-inductor boost converter generates a constant high supply voltage. This high voltage powers multiple second-stage switching amplifiers that generate custom drive waveforms required by the actuators. In designing a PEU for multiple capacitive load under stringent weight constraints, this two-stage design is advantageous in allowing multiple capacitive loads to share a single step-up converter with one magnetic component, since a single-stage converter would require one magnetic component per capacitive load.

Moreover, this design series-connects two PZT layers of a bimorph actuator in the simultaneous drive configuration, and excites each bimorph actuator with only one sinusoidal drive signal. This further reduces necessary circuitry by reducing the number of drive-stage circuits required for driving two

Manuscript received January 1, 2017; revised March 15, 2017; accepted April 27, 2017. Date of publication May 15, 2017; date of current version January 3, 2018. This work was supported in part by the NSF under Grants IIS-0926148 and CCF-1218298, and in part by the DARPA under Grant HR0011-13-C-0022. Recommended for publication by Associate Editor B. Chen. *(Corresponding author: Mario Lok.)*

M. Lok, E. F. Helbling, R. Wood, D. Brooks, and G.-Y. Wei are with the Engineering and Applied Science Department, Harvard University, Cambridge, MA 2138 (e-mail: mlok@seas.harvard.edu; ehelbling@seas.harvard.edu; rjwood@eecs.harvard.edu; dbrooks@eecs.harvard.edu; gywei@g.harvard.edu).

X. Zhang is with the Electrical and Computer Engineering Department, Washington University in Saint Louis, St. Louis, MO 63130 USA (e-mail: xuan.zhang@wustl.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2017.2704290

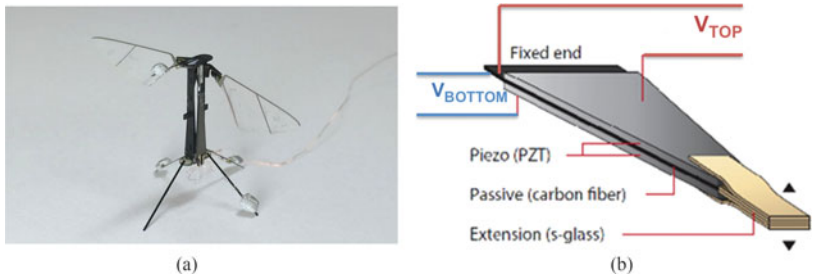


Fig. 1. (a) RoboBee is a milligram-scale flapping-wing robot with two bimorph actuators. (b) Detailed drawing of the bimorph actuator.

capacitive loads in a bimorph actuator from two to one. The switch amplifier drive stage enables bidirectional power conversion between the two capacitive loads using the output inductor as an energy storage element [7]. To further reduce weight to meet the payload budget of the robot, follow-up work builds upon this design by combining the high-voltage transistors onto a monolithic integrated circuit (IC) using a high-voltage LDMOS process [10] and limiting magnetic components to a single coupled inductor. Furthermore, push–pull drive stages avoid the need for output inductors to reduce weight, but this takes away the energy recovery capability and consequently increases PEU power consumption.

In this paper, we present a new power electronics architecture that inherits the two-stages approach, but the two capacitive loads of the bimorph actuator are parallel-connected in an alternating drive configuration. The additional drive circuitry required by this architecture is offset by the weight benefits of an IC design. Furthermore, rather than using magnetic components in the drive stage, this design exploits the symmetry of a bimorph actuator to save power while enabling energy recovery. Specifically, this new design applies three power saving features: dynamic common mode adjustment, envelope tracking (ET), and charge sharing (CS).

A novel high-side gate driver circuit designed for n-type lateral DMOS (nLDMOS) device obviates area-intensive p-type high-voltage transistors to further reduce weight of the power IC.

Finally, we demonstrate higher conversion efficiency using a boost-flyback converter that consumes weight comparable to that of a tapped-inductor boost converter used in previous designs. The rest of the paper begins by describing the electrical characteristics and drive requirements of the PZT actuators. Then, it describes the three power saving techniques dynamic common mode, ET, and CS. The remainder of the paper describes the physical implementation of the drive circuits, reviews test results, and discusses the benefits of implementing this design.

II. Background

Before delving into the proposed design, this section first reviews PZT actuator characteristics, two actuator configurations that are important to understand, and two previous actuator driver designs that are most relevant to this paper.

A. PZT Actuator Charateristics

The RoboBee employs two bimorph piezoelectric actuators to flap its two wings. As shown in Fig. 1(b), each actuator consists of a stack of PZT-5H sandwiching a carbon fiber composite layer that serves to bond the piezoelectric layers and provide a central electrical connection. The electric signal between the top and middle electrodes (V_{TOP}) excites the top PZT layer, while the signal between the middle and bottom electrodes (V_{BOTTOM}) excites the bottom PZT layer. The actuator deflects according to the differential voltage between the top and bottom layers ($V_{\mathrm{TOP}} - V_{\mathrm{BOTTOM}}$), wherein the two signals are 180° out of phase. Actuator deflection directly translates to RoboBee wing stroke, which determines the thrust force produced by the flapping wings. Each actuator layer can be modeled as a capacitive load to the driver circuits [4].

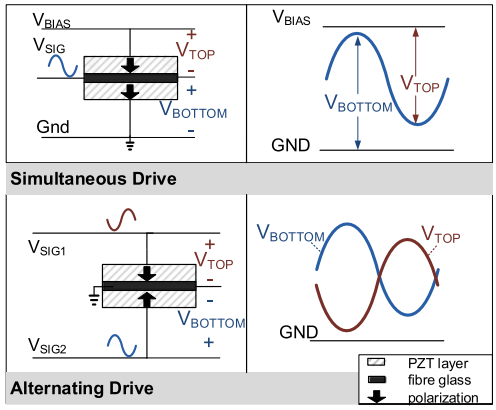


Fig. 2. There are two options to drive a bimorph PZT actuator. Simultaneous drive requires one driver connected to the middle layer. Alternating drive relies on two driver channels to generate out-of-phase sinusoids across the PZT layers with a grounded middle layer.

B. Actuator Configuration Options

Depending on the polarization direction of the PZT layers, the actuator driver can energize the actuators via a simultaneous drive or an alternating drive configuration—shown in Fig. 2 [6]. For simultaneous drive, the actuator driver provides a constant high-voltage bias (V_{BIAS}) across the series stack of the two PZT layers and a single sinusoidal signal drives the middle layer. In contrast, the alternating drive topology grounds the middle layer and drives the top and bottom PZT layers (connected in parallel) with a pair of out-of-phase sinusoids. The main distinction between these two configurations is that the PEU needs one sinusoidal output per actuator for simultaneous drive versus two for alternating drive.

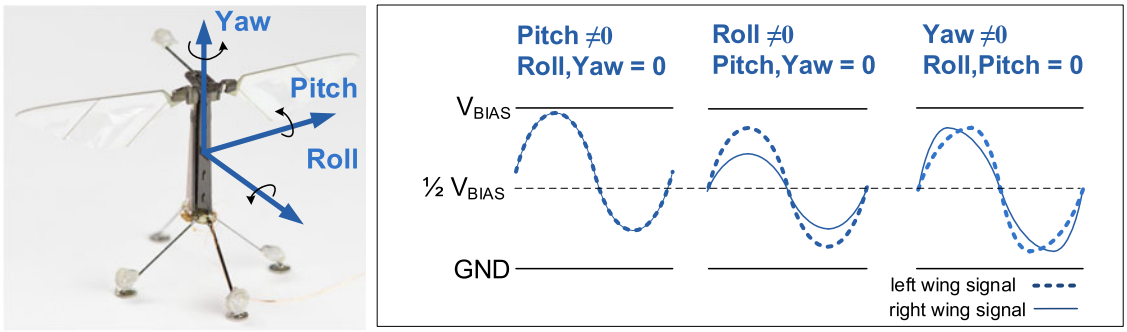


Fig. 3. This example shows the drive signals that create rotations in three axes.

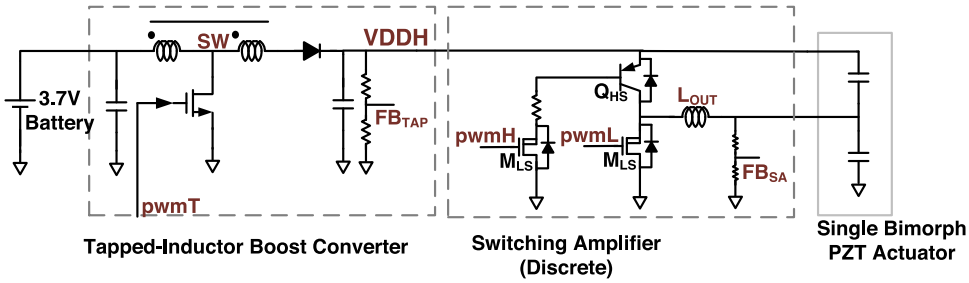


Fig. 4. Karpelson *et al.* [4] demonstrate a PEU implementation in simultaneous drive.

C. Controlling the RoboBee

The simultaneous drive configuration was first tested on the RoboBee because it requires fewer sinusoidal drive signals, minimizing parts consumption. The work in [11] designed a set of control signals that map to torque generated by the robot along roll, pitch, and yaw axes. These control signals (V_L, V_R) for the two actuators attached to the left and right wings are described by

$$V_L, V_R = [(1-\mu)\sin(2\pi ft) \pm \mu\sin(4\pi ft)] * \frac{(V_{\text{amp}} \pm V_{\text{Roll}})}{\gamma} + V_{\text{Pitch}} + \frac{V_{\text{BIAS}}}{2}. \quad (1)$$

Here, V_{amp} sets the nominal amplitude of the drive signal corresponding to average thrust. Asymmetric left and right wing stroke amplitudes (via V_{Roll}) leads to roll. Simultaneously shifting the signal dc level (via V_{Pitch}) of the left and right sinusoids leads to pitch rotation due to a shift of the mean stroke angle relative to the robot's center of mass. Finally, adding a second harmonic to the sinusoid (via μ) leads to yaw rotation due to asymmetric up and down strokes. γ is a normalization constant corresponding to μ. Examples of these sinusoidal drive signals are illustrated in Fig. 3.

The nominal thrust required by the robot translates to V_{amp} of 200 V and drive frequency f at 100 Hz. The necessary control tuning range for V_{Roll}, V_{Pitch}, and μ to guarantee a stable flight are ± 20 V, ± 50 V, and ± 0.2, respectively. The bias voltage V_{BIAS} is then set according to the inequality relation (2) such that the bias voltage is high enough to ensure the voltage across any actuator layer remain strictly positive over the control range while not exceeding the voltage rating of the electronics and the actuator at 300 V

$$(V_{\text{amp}} + |V_{\text{Roll}}| + |V_{\text{Pitch}}|) < V_{\text{BIAS}} < 300\,\text{V}. \quad (2)$$

D. PEU for the RoboBee in Prior Work

The work in [4] proposes a two-stage PEU implementation for the simultaneous drive configuration using discrete components, as shown in Fig. 4. A 15 mg output inductor enables energy recovery to reduce energy consumption by 50% compared to a push–pull linear drive stage. However, adding a second switching amplifier channel for the second actuator would push this PEU beyond the weight budget. To reduce weight, a follow-on design integrated a two-channel switching amplifier drive stage onto a single chip using high-voltage LDMOS transistors. However, the much higher parasitic C_{DS} capacitance of these transistors compared to their discrete counterparts led to higher switching losses and results in only 20% energy reduction [10]. For the RoboBee application, this 20% energy savings cannot overcome the 30 mg weight penalty associated with the two output inductors. To fit within strict weight constraints, we decided to pursue an integrated, inductor-less, push–pull drive stage, shown in Fig. 5. In both designs proposed in [4] and [10], the driving signals for the actuator are preloaded into memory, and real-time update of driving signals to roll, pitch, and yaw input were not supported.

III. Low-Power PEU Design

Building on prior work, the prospective PEU design should interface with the flight controller and generate sinusoidal driving signals accordingly. It also aims to retain the lightweight benefit of the PEU design proposed in [10] (see Fig. 5) and to achieve lower power consumption without adding prohibitive weight.

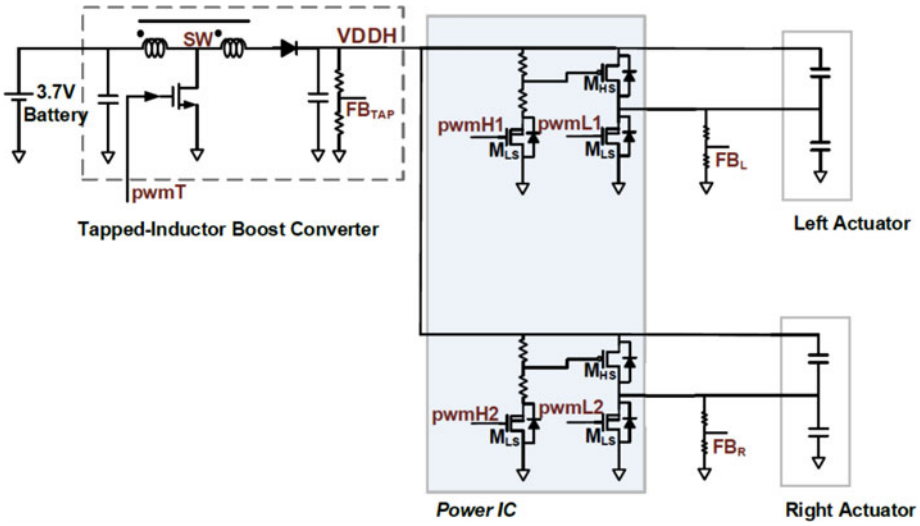


Fig. 5. Lok *et al.* [10] show a PEU with a two-channel inductor-less integrated drive stage implementing the simultaneous drive configuration.

To meet these objectives, we propose a two-stage PEU topology for the alternating drive configuration. Similar to previous work, the two-stage topology only requires a single step-up converter with one magnetic component to create an intermediate high voltage from which multiple driver circuits in the drive stage draw energy to produce individual drives signals for each of the capacitive loads. This approach yields a lower mass design than single-stage PEU designs, because single-stage designs need one magnetic component per capacitive load.

In addition, the proposed PEU implements three power-saving features—dynamic common-mode adjustment, ET, and CS. The ET feature allows power consumption of the PEU to adapt to the flight control input, making it lower on average. Although the alternating drive configuration requires twice as many drive stage channels, the additional mass and size is small thanks to monolithic circuit integration.

A. *Optimizing the Drive Waveform: Dynamic Common Mode*

First, we propose to adjust the common-mode voltage between the drive signals for the top and bottom layer of a bimorph actuator with respect to roll, pitch, and yaw control. Recall, for a bimorph actuator, the deflection is a function of the differential signal, $V_{\mathrm{TOP}} - V_{\mathrm{BOTTOM}}$, while the common mode signal $\frac{(V_{\mathrm{TOP}}+V_{\mathrm{BOTTOM}})}{2}$ does not contribute to actuator motion. Therefore, we can further optimize the driving signals, shown in Fig. 3, by reducing the common mode voltage while keeping the differential voltage constant. Fig. 6 shows the driving signals with and without common adjustment for simultaneous drive. The V_{BIAS} and the common mode voltage headroom changes with roll and pitch flight control command, labeled in Fig. 6. The minimum common mode level is constrained by the requirement that both V_{TOP} and V_{BOTTOM} need to remain positive to keep the PZT layers in contraction mode for reliability reasons. Employing the method, the driving signals is reduced in absolute voltage and therefore require less power in the drive stage.

For the alternating drive configuration, we can reuse the drive signals for the bottom layers from the simultaneous drive configuration, as shown in (3). V_{LB} and V_{RB} denote the driving signal for the bottom layers of the left and the right actuator. Then the out-of-phase driving signals for the top layers, V_{LT} and V_{RT}, can be computed via $V_{\mathrm{BIAS}} - V_{\mathrm{BOTTOM}}$, resulting in (4). Fig. 7 illustrates the differences between waveforms with and without

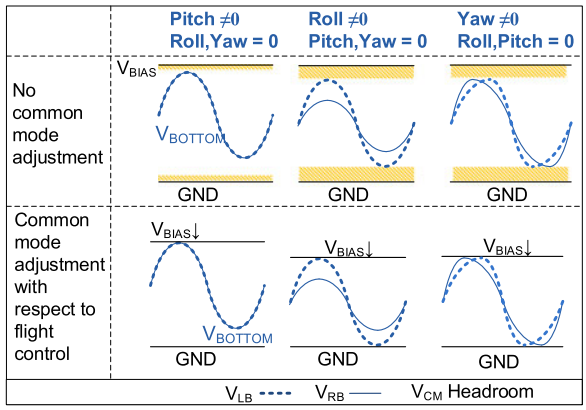


Fig. 6. Comparison between the roll, pitch, and yaw drive signals shows the adjustment to V_{BIAS} and the common mode voltage while keeping differential voltage consistent for the simultaneous drive configuration.

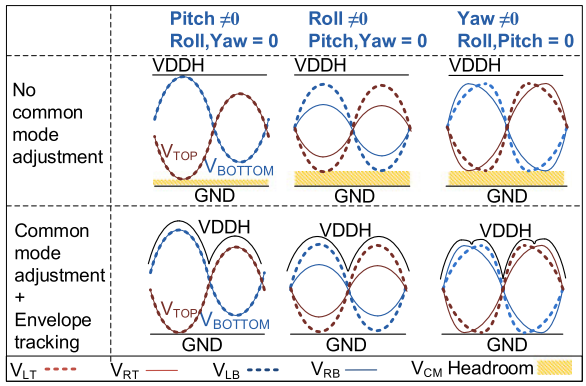


Fig. 7. Comparison between the roll, pitch, and yaw driving signals shows the adjustment to common mode voltage and ET for the alliterating drive configuration.

common-mode adjustment, all while providing roll, pitch, and yaw control.

The minimum common mode level depends on roll and pitch control and can be computed using (5). As the PEU needs to dynamically update the common mode voltage of the driving signal in real time in response to flight control command updates, we call this feature dynamic common mode

$$V_{\mathrm{LB}}, V_{\mathrm{RB}} = [(1-\mu)\sin(\omega t) \pm \mu\sin(2\omega t)] * Y \quad \frac{(V_{\mathrm{amp}} \pm V_{\mathrm{Roll}})}{\gamma} - V_{\mathrm{Pitch}} + V_{\mathrm{CM}} \tag{3}$$

$$V_{\mathrm{LT}}, V_{\mathrm{RT}} = -[(1-\mu)\sin(\omega t) \pm \mu\sin(2\omega t)] * \frac{(V_{\mathrm{amp}} \pm V_{\mathrm{Roll}})}{\gamma} - V_{\mathrm{Pitch}} + V_{\mathrm{CM}} \tag{4}$$

$$V_{\mathrm{CM}} = \frac{(V_{\mathrm{amp}} + |V_{\mathrm{Roll}}|)}{2} + |V_{\mathrm{Pitch}}|. \tag{5}$$

Lowering common mode voltage leads to simultaneous reduction in the dc level signals V_{TOP} and V_{BOTTOM}, and hence reduces the burden on the power electronics and improves the efficiency of charging the capacitive loads.

B. Envelope Tracking

The second power-saving feature in the PEU—ET—involves dynamically minimizing the supply voltage of the driver circuit based on the time-varying output waveform of the driver [12]. Recall that the simultaneous drive configuration requires a constant high-voltage V_{BIAS}, which ensures that the voltage signals across the top and bottom PZT layers are always 180° out of phase.t In contrast, the alternating drive configuration relies on two separate drive stages to independently energize the top and bottom PZT layers of the actuator. Since this topology does not require a constant high voltage bias, there is an opportunity to dynamically reduce the intermediate voltage generated by the step-up converter (V_{DDH}) while reliably generating the desired output sinusoids across the two PZT layers. The controller for the boost converter monitors output waveform requirements and appropriately sets V_{DDH}. The ET relationship between the output channels and V_{DDH} is given by

$$V_{\mathrm{DDH}} = \max\{V_{\mathrm{LT}}, V_{\mathrm{LB}}, V_{\mathrm{RT}}, V_{\mathrm{RB}}\} + V_{\mathrm{Margin}}. \tag{6}$$

ET reduces power consumption in two ways. First, it minimizes the voltage level of V_{DDH} from which current is drawn to charge the capacitive actuator loads. Second, the boost converter's efficiency improves when supplying power at a lower output voltage.

C. Charge Sharing

CS is the third power-saving feature, which seeks to reduce power by moving charge between two parallel capacitors [13]. In a linear drive stage, when discharging the capacitive load, energy is completely dissipated in the power transistors. One way to recover such energy lost is to employing CS between two capacitive loads, allowing charges to flow from the capacitor with a higher voltage potential to the capacitor with a lower voltage potential.

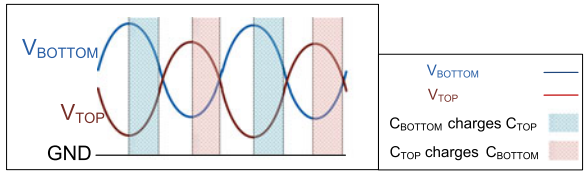


Fig. 8. Example waveform show CS is possible for half clock cycle.

CS is possible when the voltage on the capacitor to be discharged is higher than the voltage of the capacitor to be charged. When a bimorph actuator is configured in the alternating drive configuration, the sinusoidal drive signals across C_{BOTTOM} and C_{TOP} of a bimorph actuator are always 180° out of phase. Therefore, in this configuration, CS is possible for part of the sinusoidal cycle. Fig. 8 illustrates the driving signal for the top and bottom of an actuator, and the part of the cycle where CS can be applied is labeled.

IV. Drive Stage Implementation in Alternating Drive Configuration

The proposed PEU implementing the three power saving features described in Section III is shown in Fig. 9. A step-up converter generates an intermediate high-voltage supply V_{DDH}. An integrated drive stage in alternating drive configuration is implemented with two power ICs . It outputs four driving signals, and excites the top and bottom layers of two actuators individually while drawing energy from V_{DDH}. To further optimize the power and weight of the PEU, the drive stages use an nDMOS-only design and the step-up converter employs a boost-flyback converter [13]. The feedback loop of the step-up converter and the drive stage are implemented on a system-on-a-chip (SoC). Although this topology in the alternating drive configuration requires doubling the number of output channels from two to four, the incremental size and weight increase for an integrated design is small.

A. Drive Stage Implementation

Each drive stage channel consists of a high-side switch M_{HS} and a low-side switch M_{LS}. The inputs $pwmH$ and $pwmL$ control M_{HS} and M_{LS}, respectively. In each power IC, the CS switches M_{CS1} and M_{CS2} implement a CS path between the output of two channels. The turn ON of M_{CS1} and M_{CS2} are controlled by the input $pwmCS$.

B. Gate Drive Design

To save chip area and to minimize the overhead associated with introducing the ET and CS techniques, the proposed PEU in this paper uses n-type DMOS (nDMOS) transistors as high-side switches in the drive stage, which are 10× more area efficient than p-type drain-extended high-voltage transistors (pDeMOS) of equal resistance. However, one major challenge of using high-side nDMOS transistors is the design of the gate driver. The gate driver needs to generate a control signal with reference to the source of the nDMOS, V_{SW}, which follows a time-varying high-voltage sinusoid.

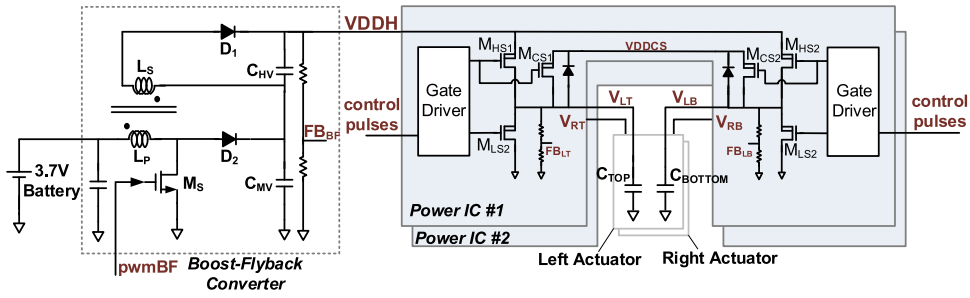


Fig. 9. Proposed PEU implementing alternating drive consists of a boost-flyback converter first stage and a four-channel ET CS drive stage.

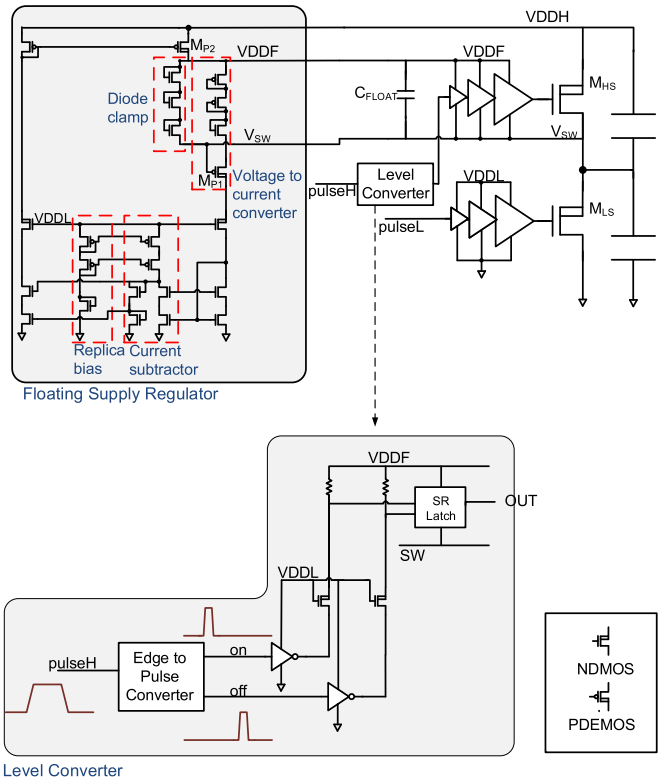


Fig. 10. Current-mode feedback loop circuit implements a floating supply regulator that powers a high-side gate driver, allowing use of high-side nDMOS transistors V_{SW}, which follows a time-varying high-voltage sinusoid.

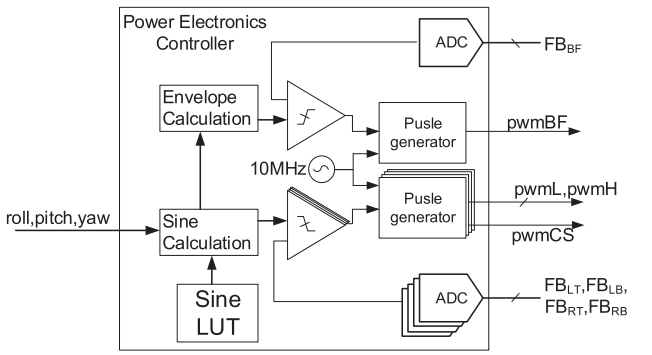


Fig. 11. Power electronics controller, as part of an digital SoC, implements the feedback loop for the drive stage and the step-up converter .

A conventional bootstrapped gate driver maintains a floating supply with a stable voltage relative to V_{SW} by charging the floating supply from the low-voltage supply via a bootstrapped diode when V_{SW} reaches 0 V. The floating supply, decoupled with a floating capacitor, powers a level converter that translates a low-voltage signal to the floating supply domain, and powers gate drive buffers that turn ON and OFF the nDMOS directly. The bootstrapped diode approach to recharge the floating capacitor is not suitable for this application as V_{SW} does not return to 0 V at every switching cycle the way traditional half-bridge switcher does.

In this paper, we inherit the approach of using a floating supply to power the gate drive buffers and a level-converter for the high-side nDMOS, however powers the floating supply (V_{DDF}) with the high-voltage supply V_{DDH} and regulate it through a current-mode feedback circuit (see Fig. 10). In the current-mode feedback circuit, the pDeMOS M_{P1} serves as a voltage-to-current converter that translates voltage on the floating capacitor $C_{FLOATING}$ to a current signal. The current signal is then inverted via a current-mode subtractor and delivered to a current mirror that modulates the source-to-drain current of pDeMOS M_{P2}. The current through M_{P2} charges the floating capacitor $C_{FLOATING}$, and regulates the floating supply 4 V above V_{SW}. Simulation shows that the maximum voltage ripple on the floating supply over process-voltage-temperature (PVT) is 2.6 V, and the minimum voltage regulation voltage for the floating supply is at 3.4 V, which sufficient to maintain the correct operation of the floating supply.

The source degeneration of M_{P1} with three diode-connected transistors improves sensitivity of voltage-to-current conversion, and minimizes the always-ON sensing current through M_{P1} ($22\,uA$). The level-converter first converts input into set and reset pulses before using these pulses to program an SR-latch in the floating supply domain, minimizing the static current consumed in the level-translation process. The float supply decouple capacitor, sized at 3 pF is implemented with MOS caps in an isolated high-voltage N-Well.

C. Drive Stage Control

The output of the drive stage tracks sinusoidal driving signals that represent roll, pitch, and yaw rotations, while the boost-flyback converter output is maintained as an envelope of the four driving signals. The feedback loop that realizes these driving signal waveform, shown in Fig. 11, are part of an SoC in TMSC 40 nm process [14]. In 10 us interval, resistor divided versions of the driving signals are sampled by an SoC via four 8-bit ADC channels at 100 kHz, and they are compared against digital references computed by the sine compute block according

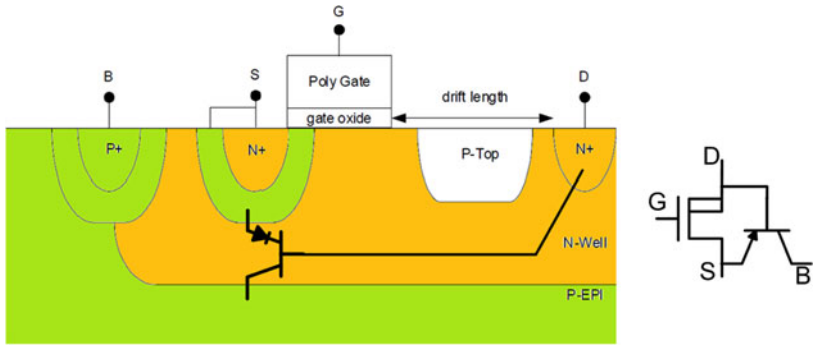


Fig. 12. Source P-diffusion, high-voltage N-well and P-type substrate forms a parasitic p-n-p device that leaks energy to the substrate when the source to drain diode turns ON.

to (3) and (4). The drive stage feedback controller implements a pulse swallow modulation scheme, in which case the pulse generator nominally outputs a 300 ns pulse at 100 kHz, and the pulse is either gated or passed to pwmL and pwmH depends on the outcome of the comparator. Effectively, for each driving channel, during the rising half of a sinusoid, the power electronics controller momentarily turns ON $M_{\rm HS}$ via pwmH when the driving signal trails the reference. Similarly if the driving signal trails the reference in falling half, the controller pulses pwmL to discharge the output capacitive load.

To implement ET, the controller samples $V_{\rm DDH}$ via a fifth ADC channel sampling at 200 kHz, twice the sampling frequency of other four ADC channels. The sampled $V_{\rm DDH}$ is then compared against the envelope voltage reference, computed based on the driving signals. Similar to the drive stage feedback loop, the boost-flyback converter controller also utilizes a pulse swallow modulation scheme. When $V_{\rm DDH}$ is smaller than the envelope voltage, the controller pulses the switch M_S to initiate an energy conversion cycle for the boost-flyback converter. When $V_{\rm DDH}$ lags the envelope voltage, the boost-flyback converter has a maximum switching frequency of 200 kHz and it is effectively pulse-frequency modulated depends on the power drawn by the drive stage.

The controller also monitors opportunities for CS and selectively turns ON the direct conduction path between $C_{\rm TOP}$ to $C_{\rm BOTTOM}$ by controlling the CS switches $M_{\rm CS1}$ and $M_{\rm CS2}$. When the feedback loop detects that the drive stage needs to discharge a capacitor load with a higher voltage and charge the other capacitor in the actuator with a lower voltage, or in other words when the inequality 7, 8, and 9 are met, the controller turns ON $M_{\rm CS1}$ and $M_{\rm CS2}$ to charge share the two capacitor loads instead of turning ON the $M_{\rm HS}$ and $M_{\rm LS}$ transistors individually for charging and discharge the two capacitor loads

$$\frac{dV_{\rm LTREF}}{dt} > 0 \text{ and } V_{\rm LT} < V_{\rm LTREF} \tag{7}$$

$$\frac{dV_{\rm LBREF}}{dt} < 0 \text{ and } V_{\rm LB} > V_{\rm LBREF} \tag{8}$$

$$V_{\rm LB} > V_{\rm LT}. \tag{9}$$

Unfortunately, when CS is used in this process, parasitic p-n-p transistors (see Fig. 12), connected to the body diodes of these CS switches, turn ON and draw away approximately 80% of the charge to the substrate, leaving only 20% to charge up the other capacitor. Thus, this feature was much less effective than originally simulated. The problematic parasitic transistor comes from the shared substrate in the bulk DMOS process used, however, future high-voltage silicon-on-insulator processes will not have this problem.

D. Step-up Converter Design

The step-up converter of the proposed PEU uses a boost-flyback converter implementation [15]. With this design, we achieved higher efficiency for output voltage above 100 V and incurs small weight overhead. In addition, this converter operates with higher efficiency than prior PEU implementing simultaneous drive also because the power saving techniques applied in the drive stage lower the average output voltage required for step-up converter.

The boost-flyback converter consists of a flyback converter and an auxiliary boost converter. The output voltage is the sum of the flyback converter output and the auxiliary boost converter output, as the outputs of these two subconverters are series-connected (see Fig. 9). The auxiliary boost converter serves as a snubber circuit and clamps the switch node. Compared to the snubber-less tapped-inductor boost converter used in previous designs [4], [10], this converter requires one additional capacitor and diode rated for 50 V ($C_{\rm MV}$ and D_2). The extra diode will incur additional conduction loss. However, we achieve higher efficiency with this converter topology for three reasons. First the auxiliary boost converter prevent the energy stored in the primary-side leakage inductance from dissipating through LR ringing of the switch node, and instead directs this energy to the output. Second, it reduces the voltage stress on the high-voltage capacitor $C_{\rm HV}$ and the high-voltage diode D_1. Third, it alleviates the efficiency loss associated with the parasitic capacitance of the flyback converter rectifier. At the end of a conversion cycle, after the current in the secondary winding is fully discharged via the rectifying diode, energy is drawn from the output to charge the parasitic capacitance of the diode. This energy is proportional to the square of the voltage seen by the diode D_1 in the off-cycle. For a boost-flyback converter, since the diode D_1 sees only a fraction of the converter output voltage, the parasitic capacitance of D_1 has a smaller impact.

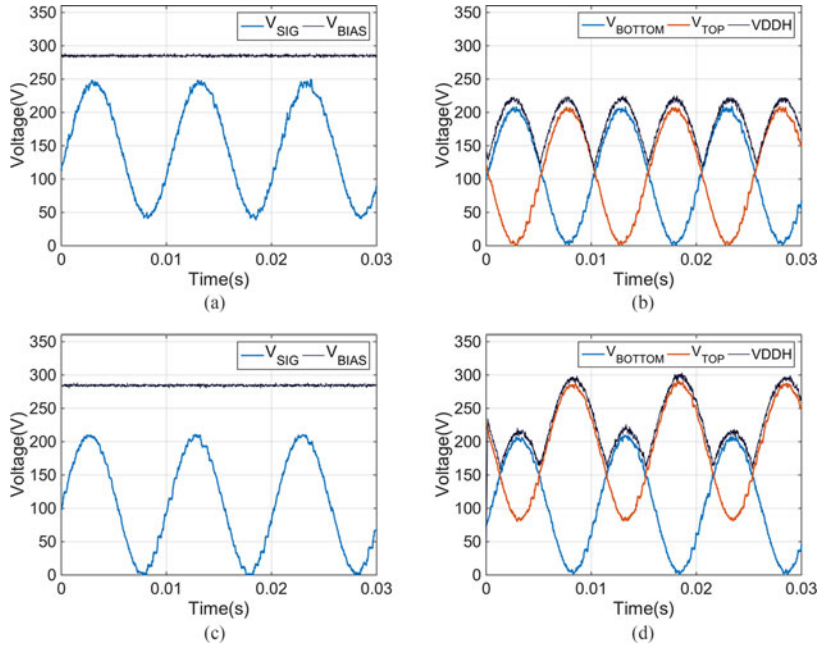


Fig. 13. Experimental measurement shows the drive signal difference for a single actuator between simultaneous drive and alternating drive for two different control settings. (a) Simultaneous Drive - V_{Roll}, V_{Pitch}, and μ_{yaw} all equal to 0; (b) Alternating Drive - V_{Roll}, V_{Pitch}, and μ_{yaw} all equal to 0; (c) Simultaneous Drive - V_{Roll}, and μ_{yaw} equal to 0; $V_{\mathrm{Pitch}} = 40$ V; (d) Alternating Drive - V_{Roll}, and μ_{yaw} equal to 0; $V_{\mathrm{Pitch}} = 40$ V.

V. Test Results

To demonstrate the power saving features described above, we tested and compared the prior PEU design, shown in Fig. 5, in simultaneous configuration and the proposed design, shown in Fig. 9, in alternating drive configuration. Four 15 nF capacitors representing the two bimorph actuators are driven at 100 Hz, 200 V_{PP} excitation waveforms.

A. Functional Validation of Drive Stage

The scope capture shown in Fig. 13(a) and (b) show drive waveform output that corresponding to zero pitch rotation for an actuator in simultaneous drive configuration and alternating drive configuration, respectively. Fig. 13(c) and (d) show the scenario for $V_{\mathrm{Pitch}} = 40$ V. This verifies proper operation of the ET and dynamic common mode adjustment features for two drive channels of a single actuator. Fig. 13(b) and (d) also show that the flight control input impacts the ET waveform and the possible common mode adjustment, and hence impact the overall power consumption of the PEU. The measurements that quantify this dependence are shown later.

Fig. 14 shows the drive signal V_{TOP} and V_{BOTTOM} in the frequency domain in comparison to a perfect 100 Hz 200 Vpp sinusoid. The measured total harmonic distortion (THD) for these two driving signals is at 3%. This result verify that the PEU can generate out-of-phase sinusoids needed to excite the top and bottom layer of an actuator in the alternating drive configuration.

B. Gate Driver Evaluation

Fig. 15 shows the measured voltage signal of V_{DDF}, SW, the voltage across the floating capacitor $V_{\mathrm{DDF}} - \mathrm{SW}$, and the control signal pwmH for a short segment of the sinusoidal drive cycle.

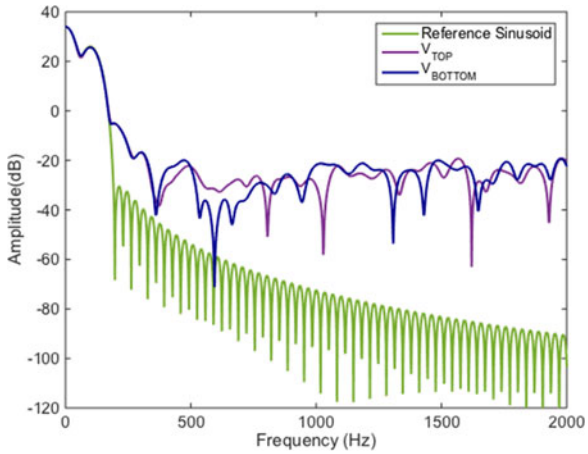


Fig. 14. Frequency spectrum of driving signals in Fig. /refscopeB is compared visually against the ideal sinewave. The THD of driving signals is computed to be 3%.

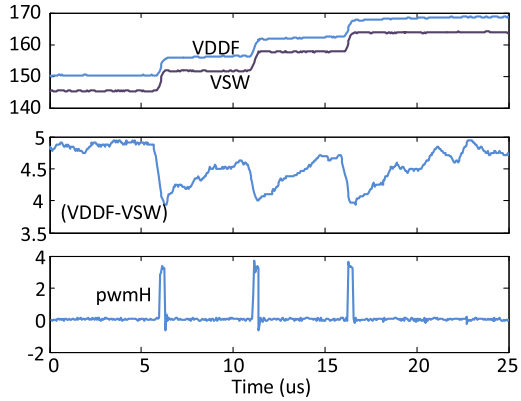


Fig. 15. Transient snapshot of the voltage node V_{DDF}, SW, and pwmH shows the floating supply is regulated above 4 V as the SW node follows a 200 V sinusoid trajectory.

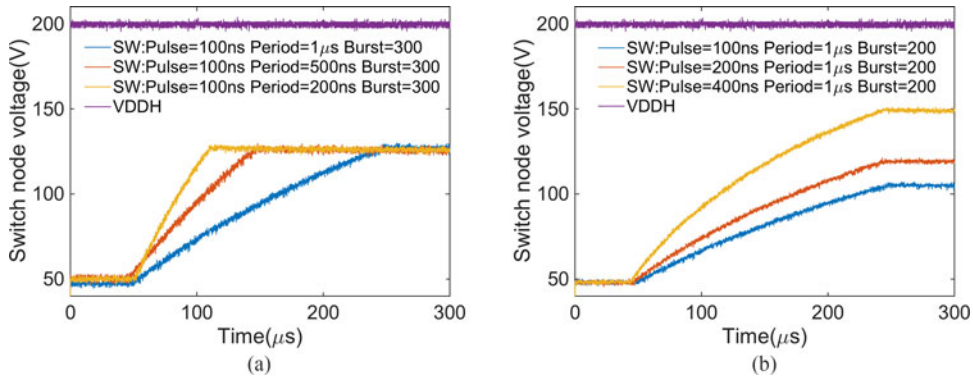


Fig. 16. To excise the extend of the capability for the floating supply, we experiment with a burst of pulse at larger pulse width and high pulse frequency. (a) Sweep pulse frequency, (b) Sweep pulse width.

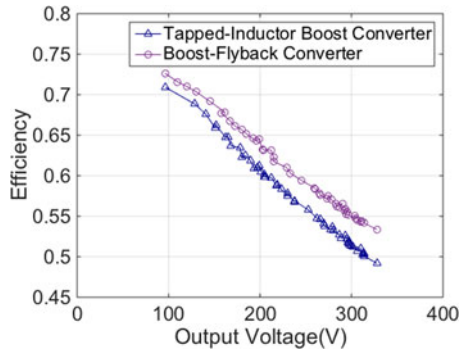


Fig. 17. Step-up converter efficiency measurement shows the Boost-Flyback Converter yields 3% efficiency improvement across a large voltage range.

This result validates that as SW follows a sinusoid signal, the voltage on C_{FLOATING} is maintained above 4 V. One limit in this floating supply design is that when pwmH is driven at a high frequency, the current drawn by the level converter and the buffer may collapse the floating supply. To demonstrate the high-side gate driver in this design can operate across a wide range of pulse frequencies (1, 2, 5 MHz) and pulse width (100, 200, 400 s), we setup an open-loop experiment where a burst of pulses drive the high-side nDMOS to charge a 100 nF capacitor at the output. Fig. 16 and (a) shows that the floating supply can sustain these pulses at different pulse width and pulse frequency settings.

The efficiency of this floating supply regulator at any given point of time is determined by the ratio $(V_{\text{DDF}} - V_{\text{SW}})/(V_{\text{DDH}} - V_{\text{SW}})$. Although the efficiency of the floating supply is low, the power dissipation of the entire high-side gate drive circuit only accounts for a small percentage of the total power consumption. In the case where the PEU drives 15 nF capacitive loads with 100 Hz 200 V peak-to-peak sinusoids, the power consumption of the high-side gate drivers is estimated to be 5% of the total power in simulation.

C. Step-up Converter Evaluation

Fig. 17 shows the measured efficiency comparison the tapped-inductor boost converter and the boost-flyback converter as a function of output voltage at 300 mW output power. The boost-flyback converter has consistently higher efficiency than the tapped-inductor boost converter across the voltage range 100–300 V.

To estimate the efficiency improvement for the converter to output V_{DDH} as an envelope voltage, as opposed to a constant bias voltage of 280 V, we review two examples where the envelope voltages are different.

Since the envelope voltage depends on the roll, pitch, and yaw control settings, we chose the zero rotation scenario representing the best case and pitch-at-40 V scenario representing the worst case. The average efficiency for the case of the zero rotation is 67%, better than a 280 V bias 11%. The average efficiency of the case for pitch $=$ 40 V is 61%, which translates to 5% efficiency improvement.

D. System Evaluation

The drive stage and step-up converter measurements show that benefit of the power saving techniques are different for zero rotation and nonzero rotation. To quantify the dependence of the PEU power and the power savings on roll, pitch, and yaw rotation, the PEU power are measured at various control setting, shown in Fig. 18. To show the impact of each rotation, only one of roll, pitch, and yaw is swept while the other two are kept at 0 in each test. However, in an actual flight test, any combinations of the three rotation torque command can be nonzero. The power consumption of the proposed design in alternating drive utilizing ET, CS, dynamic common mode voltage (Dynamic VCM) is compared against the baseline linear driver implementing the simultaneous drive configuration. With the three power techniques, up to 48% power reduction is achieved over the prior design presented in [10].

To evaluate the PEU in an experiment that emulates an actual flight, we configure the PEU to excite four 15 nF capacitive loads with nominal 200 Vpp and 100 Hz driving signals while tracking a 2.5 s roll, pitch, and yaw trace recorded from a RoboBee hovering experiment, plotted in Fig. 19. Fig. 20 shows the measured driving signals of V_{LB}, V_{LT}, V_{RB}, and V_{RT} from this benchmark, validating the driving signal follows the roll, pitch, and yaw controls. This benchmark shows that in a hovering flight, the deviation of pitch, which has the highest impact on power consumption, is small. Hence, power saving techniques utilized in this PEU is effective most of the time. The distribution of power consumption for the step-up converter over different

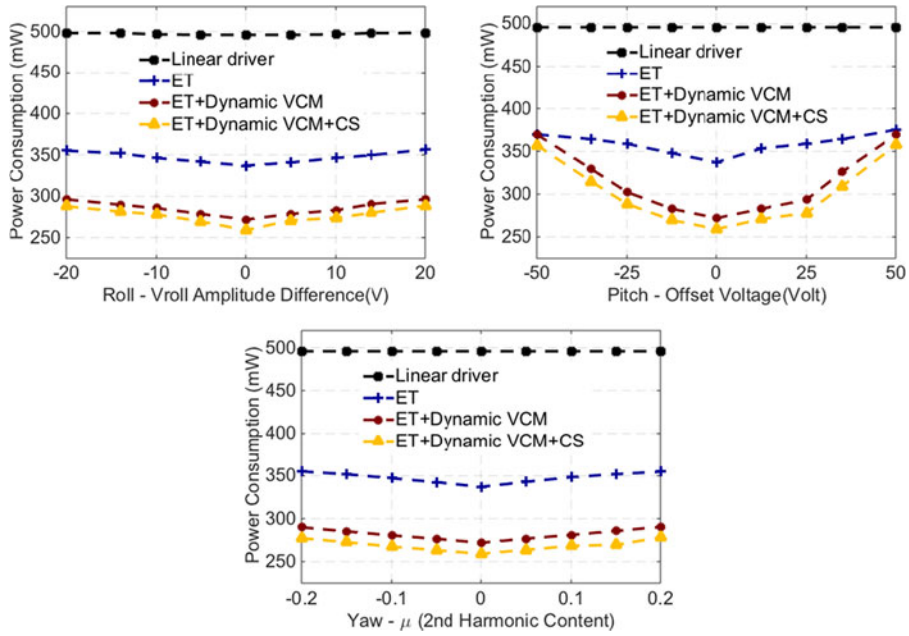


Fig. 18. Total power consumption changes depending on roll, pitch, and yaw commands.

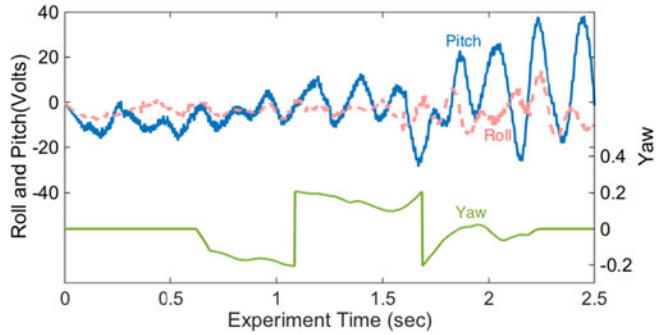


Fig. 19. 2.5 s roll, pitch, and yaw flight recording is used as a benchmark to evaluate the power saving achieved with proposed PEU design.

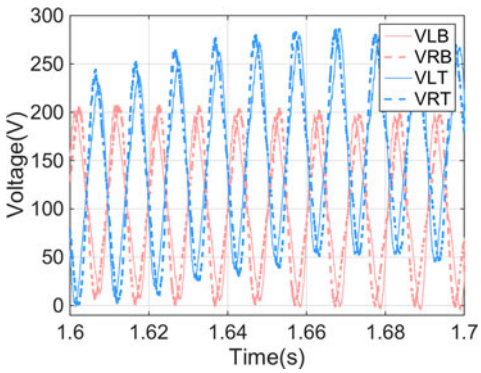


Fig. 20. Drive signals of all four actuator layers corresponding to a segment of the benchmark shows the drive signals respond to control changes.

voltage ranges, shown in Fig. 21, also reasserts that the step-up converter of the proposed PEU mostly operates in the more efficient output voltage range, as compared to previous design. The average power of PEU tracking this benchmark is 290 mW, 37% less than the power consumed by a PEU that uses linear push–pull drive stages.

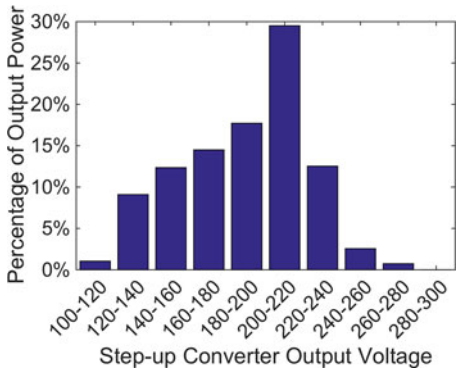


Fig. 21. Based on the benchmark, the distribution of power consumption for the boost-flyback converter over different voltage ranges shows that the medium output voltage required from the boost-flyback converter is indeed much smaller than the bias voltage in simultaneous driver configuration.

To test this PEU design for boarder applications, we measure total power consumption of the PEU at zero roll, pitch, and yaw across a range of excitation frequencies, capacitor loads, and output sine wave amplitudes, shown in Fig. 22. These results verify that the proposed design can support a wide range of applications with different output power and actuator characteristics. The amount of power it takes to charge the capacitive load in half a cycle P_{REACTIVE} given by (10), is plotted along the PEU power consumption as a reference.

Since P_{REACTIVE} is purely a function of actuator parameters and operating conditions. the ratio $P_{\text{PEU}}/P_{\text{REACTIVE}}$ is a good metric for evaluating the power efficiency of the PEU design

$$P_{\text{REACTIVE}} = \frac{1}{2} C_{\text{ACT}} V_{\text{PP}}^2 f \tag{10}$$

$$\frac{P_{\text{PEU}}}{P_{\text{REACTIVE}}} = \frac{\left(\frac{1}{\eta_{\text{DELIVER}}} - \eta_{\text{RECOVER}}\right)}{\eta_{\text{STEP-UP}}}. \tag{11}$$

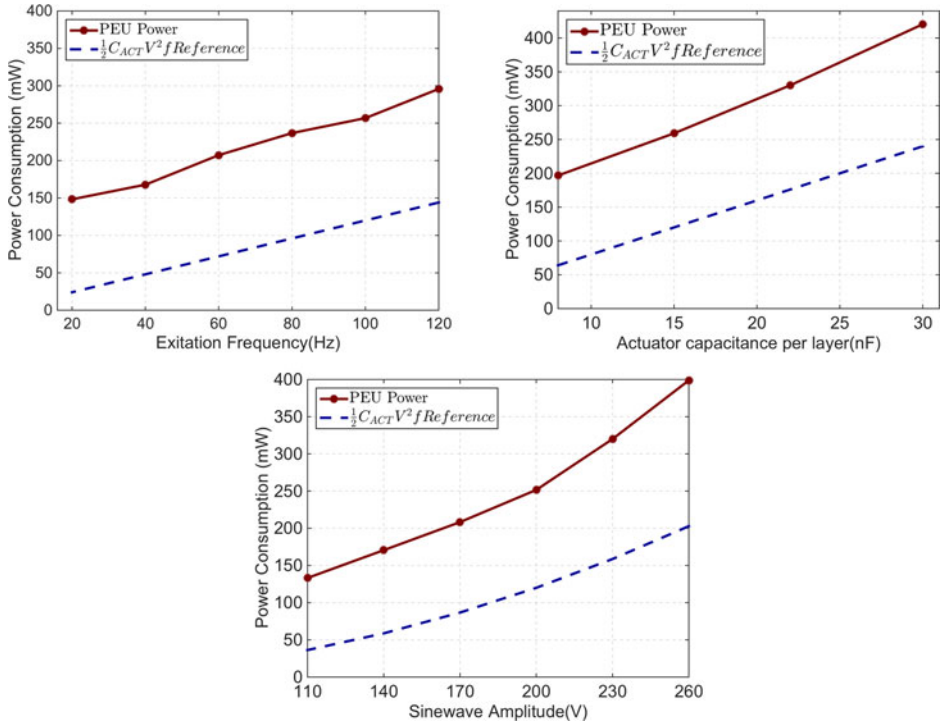


Fig. 22. Total power consumption scales with excitation frequency, actuator capacitance, and sinusoidal drive signal amplitude. The power delivered to the load for each case is plotted as a reference. (a) $C_{\mathrm{LAYER}} = 10$ nF, $V_{\mathrm{amp}} = 200$ V, sweeping f; (b) $V_{\mathrm{amp}} = 200$ V, $f = 100$ Hz, sweeping C_{LAYER}; (c) $C_{\mathrm{LAYER}} = 10$ nF, $f = 100$ Hz sweeping V_{amp}.

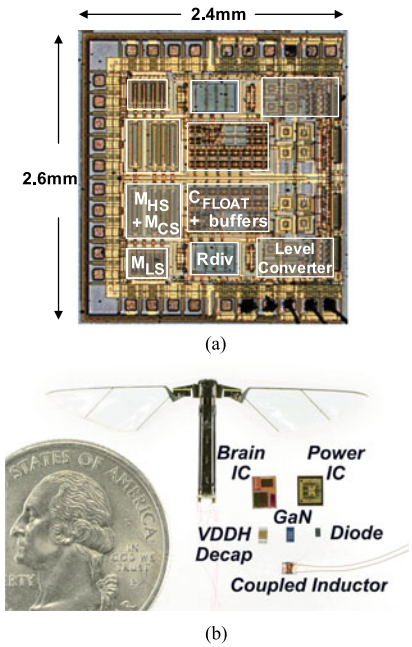


Fig. 23. (a) Chip photograph for the power IC shows the area occupied by the nDMOS switches and the gate drivers. (b) Photo shows the relative size of components used in the power electronics prototype including the custom developed power IC.

For a two-stage topology, this ratio is also related to the average efficiency of the step-up converter $\eta_{\mathrm{STEP-UP}}$, the average efficiency of energy delivery to the load η_{DELIVER}, and the average efficiency of energy recovery from the load η_{RECOVER}, as described in (11).

Last, Fig. 23(a) presents a die photo of the power IC that integrates a two-channel ET and CS drive stage, and Fig. 23(b) shows the size comparison between the RoboBee and different components of the PEU.

VI. Conclusion

This paper presents a new power electronics architecture for energizing two PZT bimorph actuators of the RoboBee. This design, optimized for both high power efficiency and low mass, consists of a boost-flyback converter step-up stage and a drive stage with multiple channels. The boost-flyback converter in the new architecture achieves 3% higher efficiency than the tapped-inductor boost converter used in previous design. Building upon an integrated inductor-less push–pull drive stage, three power savings proposed in this paper, ET, dynamic common mode, and CS, combine to reduce the drive stage power consumption by 30%–47% depends on maneuver control of the robot. A nDMOS only design with integrated high side driver further improves the area efficiency of drive stage and meet the weight constraints of RoboBee. Based on a 2.5 s maneuver control recording from a flight experiment, the proposed PEU consumed on average 290 mW while tracking the roll, pitch, and yaw command, 37% less than alternative design that meets the weight constraint.

Acknowledgements

The authors would like to thank TSMC's university shuttle program for chip fabrication.

REFERENCES

[1] K. Y. Ma, P. Chirarattananon, S. B. Fuller, and R. J. Wood, "Controlled flight of a biologically inspired, insect-scale robot," *Science*, vol. 340, no. 6132, pp. 603–607, 2013.

[2] M. Karpelson, J. P. Whitney, G.-Y. Wei, and R. J. Wood, "Energetics of flapping-wing robotic insects: Towards autonomous hovering flight," in *Proc. 2010 IEEE/RSJ Int. Conf., Int. Robot. Syst.*, 2010, pp. 1630–1637.

[3] K. Y. Ma, S. M. Felton, and R. J. Wood, "Design, fabrication, and modeling of the split actuator microrobotic bee," in *Proc. 2012 IEEE/RSJ Int. Conf. Int. Robot. Syst.*, 2012, pp. 1133–1140.

[4] M. Karpelson, G.-Y. Wei, and R. J. Wood, "Driving high voltage piezoelectric actuators in microrobotic applications," *Sens. Actuators A, Physical*, vol. 176, pp. 78–89, 2012.

[5] N. T. Jafferis, M. A. Graule, and R. J. Wood, "Non-linear resonance modeling and system design improvements for underactuated flapping-wing vehicles," in *Proc. 2016 IEEE Int. Conf., Robot. Autom.*, 2016, pp. 3234–3241.

[6] M. Karpelson, G.-Y. Wei, and R. J. Wood, "Milligram-scale high-voltage power electronics for piezoelectric microrobots," in *Proc. 2009 IEEE Int. Conf., Robot. Autom.*, 2009, pp. 2217–2224.

[7] M. Karpelson, J. P. Whitney, G.-Y. Wei, and R. J. Wood, "Design and fabrication of ultralight high-voltage power circuits for flapping-wing robotic insects," in *Proc. 2011 26th Annu. IEEE, Appl. Power Electron. Conf. Expo.*, 2011, pp. 2070–2077.

[8] C. Chen, Y. Tang, A. Khaligh, and R. W. Newcomb, "A low-power and high-gain converter for driving dielectric elastomer actuators," in *Proc. 2013 28th Annu. IEEE, Appl. Power Electron. Conf. Expo.*, 2013, pp. 2755–2760.

[9] P. Thummala, Z. Zhang, M. A. Andersen, and D. Maksimovic, "Digital control of a high-voltage (2.5 kv) bidirectional dc-dc converter for driving a dielectric electro active polymer (deap) based capacitive actuator," in *Proc. 2014 IEEE Energy Convers. Congr. Expo.*, 2014, pp. 3435–3442.

[10] M. Lok, D. Brooks, R. Wood, and G.-Y. Wei, "Design and analysis of an integrated driver for piezoelectric actuators," in *Proc. 2013 IEEE Energy Convers. Congr. Expo.*, 2013, pp. 2684–2691.

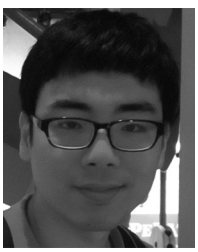
[11] P. Chirarattananon, K. Y. Ma, and R. J. Wood, "Adaptive control for takeoff, hovering, and landing of a robotic fly," in *Proc. 2013 IEEE/RSJ Int. Conf. Int. Robot. Syst.*, 2013, pp. 3808–3815.

[12] F. Wang, A. Ojo, D. Kimball, P. Asbeck, and L. Larson, "Envelope tracking power amplifier with pre-distortion linearization for wlan 802.1 1 g," *Simulation*, vol. 3, pp. 1543–1546, 2004.

[13] J. L. McCreary and P. R. Gray, "All-mos charge redistribution analog-to-digital conversion techniques. I," *IEEE J. Solid-State Circuits*, vol. 10, no. 6, pp. 371–379, Dec. 1975.

[14] X. Zhang *et al.*, "A multi-chip system optimized for insect-scale flapping-wing robots," in *Proc. IEEE Symp. VLSI Circuits Dig. Tech. Papers*, 2015, pp. 152–153.

[15] T.-J. Liang and K. Tseng, "Analysis of integrated boost-flyback step-up converter," *IEE Proc.-Elect. Power Appl.*, vol. 152, no. 2, pp. 217–225, 2005.



Mario Lok received the B.Sc. degree in engineering physics from the University of British Columbia, Vancouver, BC, Canada, in 2008 and the M.S. degree in electrical engineering from the University of Texas, Austin, TX, USA, in 2010. He is currently working toward the Ph.D. degree at Harvard University, Cambridge, MA, USA, pursuing research on miniature power electronics design on micro-air-vehicle.

His boarder research interests include power integrated circuits, switch-mode power electronics, robotics, and highly integrated electrical mechanical system.

Elizabeth Farrell Helbling received the B.S. degree in engineering sciences from Smith College, Northampton, MA, USA, in 2012. She is currently working toward the Ph.D. degree in engineering sciences at John A. Paulson School of Engineering and Applied Sciences, Harvard University, Cambridge, MA.

Her research interests include microrobotics, sensing, and autonomy. Ms. Helbling received a National Science Foundation Graduate Research Fellowship in 2013.

Robert Wood (M'01) received the M.S. and Ph.D. degrees from the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA, USA, in 2001 and 2004, respectively.

He is currently the Charles River Professor of Engineering and Applied Sciences in Harvard John A. Paulson School of Engineering and Applied Sciences, a Founding Core Faculty Member of the Wyss Institute for Biologically Inspired Engineering, Harvard University, Cambridge, MA, USA, and a National Geographic Explorer. His current research interests include microrobotics, soft and wearable robots, and bioinspired robotics.

Xuan Zhang (S'08–M'15) received the B.Eng. degree in electrical engineering from Tsinghua University, Beijing, China, in 2006, and the M.S. and Ph.D. degrees in electrical and computer engineering from Cornell University, Ithaca, NY, USA, in 2009 and 2012, respectively.

She is an Assistant Professor in the Preston M. Green Department of Electrical and Systems Engineering, Washington University, St. Louis, MO, USA. She works across the fields of VLSI, computer architecture, and robotics. Her research interests include adaptive learning hardware for autonomous systems, hardware/software codesign of efficient power delivery and distribution, and ubiquitous self-powered IoT devices.

David Brooks received the B.S. degree in electrical engineering from the University of Southern California, Los Angeles, CA, USA, and the M.A. and Ph.D. degrees in electrical engineering from Princeton University, Princeton, NJ, USA. His research interests include resilient and power-efficient computer hardware and software design for high-performance and embedded systems.

Prof. Brooks received several honors and awards including the ACM MauriceWilkes Award, the ISCA Influential Paper Award, the NSF CAREER award, the IBM Faculty Partnership Award, and the DARPA Young Faculty Award.

Gu-Yeon Wei received the B.S., M.S., and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 1994, 1997, and 2001, respectively.

He is a Gordon McKay Professor of Electrical Engineering And Computer Science in John A. Paulson School of Engineering and Applied Sciences, Harvard University, Cambridge, MA, USA. His research interests span multiple layers of a computing system: digital and mixed-signal integrated circuits, computer architecture, and design tools for efficient hardware. His research interest focuses on identifying synergistic opportunities across these layers to develop energy-efficient solutions for a broad range of applications from flapping-wing microrobots to warehouse scale computing to deep learning on edge devices.