A Fully Integrated Battery-Connected Switched-Capacitor 4:1 Voltage Regulator with 70% Peak Efficiency Using Bottom-Plate Charge Recycling

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***Abstract*—This work presents a switched-capacitor (SC) DC-DC voltage regulator that converts a 3.7V battery voltage down to ~0.8V in order to power the 'brain' SoC of a flapping-wing microrobotic bee. A cascade of two 2:1 SC converters offers high efficiency for a 4:1 conversion ratio. A charge recycling technique reduces the flying capacitor's bottom-plate parasitic loss by 50% and overall conversion efficiency reaches 70%. The output droop is less than 10% of the nominal output voltage for a worst-case 47mA load step.**

I. INTRODUCTION

In the aerial microrobotic bee application [1], the on-board battery (~3.7V) is the only source of energy. A digital SoC, which works as the 'brain' of the robotic bee, operates at low voltages (~0.8V or less). While a voltage regulator is required to bridge the voltage difference, the stringent weight and area requirements of the robotic bee make the regulator design challenging. First, the regulator needs to be fully integrated along with the SoC without using any external components in order to minimize weight and area. Second, the regulator must directly connect to the battery and support a high (4:1) step down ratio. Third, high conversion efficiency is important to achieve long flight times for the robotic bee.

SC converters are well suited for this application from weight and area perspectives since they only require capacitors and MOS transistors. On-chip MOS capacitors with density as high as 10nF/mm^2 are available in digital CMOS processes [2]. However, choosing the right topology is important. Single-stage SC converters suffer from power switch voltage breakdown and high bottom-plate parasitic loss when the conversion ratio and input voltage are high [2][4][5]. One solution has been to cascade thick-oxide transistors to avoid transistor break down in 3:1 SC converters [2][5], but this degrades conversion efficiency. Novel switching techniques have also been shown to mitigate flying capacitor bottom-plate parasitic loss [4][8]. Unfortunately, these issues get worse in single-stage 4:1 SC converters.

This paper presents a fully integrated two-stage SC regulator to address these challenges. The proposed two-stage topology simplifies the overall design and implements several techniques to improve conversion efficiency: (1) it uses the appropriate flavor of transistors (thin oxide and think-oxide transistors) in each stage; (2) it applies a charge recycling technique to mitigate bottom-plate parasitic loss; and (3) it employs separate low-boundary feedback controls to regulate the each stage's output to desired levels. Lastly, the two-stage topology provides an intermediate voltage for use by other parts of the microrobotic bee.

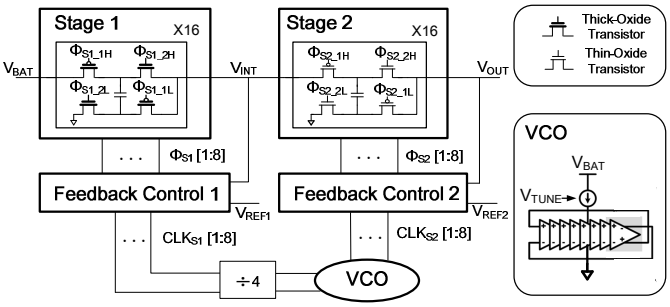

Fig. 1: Block diagram of proposed two-stage SC converter.

II. PROPOSED TWO-STAGE CONVERTER

A. Two-Stage Structure

Fig. 1 illustrates the system block diagram of the proposed SC converter. The design cascades two 2:1 SC stages, which are implemented and optimized for different purposes. The first stage converts the 3.7V battery voltage down to a 1.8V intermediate voltage (V_{INT}). To handle the 1.8V swing, this stage uses thick-oxide transistors available in the process. The second stage converts the intermediate 1.8V down to ~0.8V for the final output (V_{OUT}) using thin-oxide transistors. Each stage also includes identical, but separate feedback control loops, discussed later.

The two SC stages are nearly identical except for the type of transistors and sizing. Each SC stage implements a multi-phase topology to reduce voltage ripple. Sixteen modules operate off both edges of eight interleaved clock phases. A multi-phase current-starved pseudo-differential VCO generates the clock edges and operates directly off of the battery to guarantee proper start-up. To ensure there is always a balanced number of modules in operation, pairs of modules operate 180° out-of-phase off of one shared clock phase. SC converters have two basic phases of operation, thoroughly discussed in [2]. In one phase, energy drawn from the input charges the flying capacitor up and flows to the load. In the other phase, energy stored on the capacitor during the previous phase flows to the load. The power switches operate with stacked voltage domains similar to [3] and [6]. Taking the first-stage as an example, switches driven by Φ_{S1_1H} and Φ_{S1_2H} operate in the high voltage domain (between V_{INT} and V_{BAT}) while switches driven by Φ_{S1_1L} and Φ_{S1_2L} operate in the low voltage domain (between ground and V_{INT}).

The maximum switching frequencies of the two stages are also different. The first-stage maximum switching frequency is one quarter of that in the second stage. By doing this, the two stages occupy similar chip area and have similar conversion efficiencies, resulting in optimal overall efficiency and power density for the regulator. By optimizing the two stages separately, the first stage connects to the high battery voltage,

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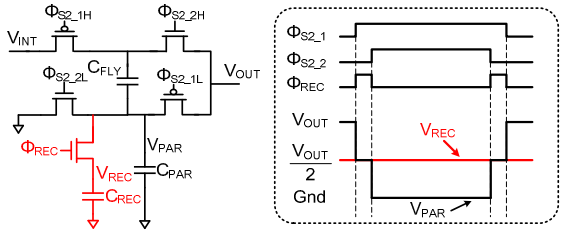


Fig. 2: Charge recycling technique and timing diagrams

but is decoupled from output load transients. The higher switching frequency of the second stage enables higher closed-loop bandwidth for fast output load transient response.

Cascading two 2:1 SC stages offers other advantages. V_{INT} and V_{OUT} can serve as stacked supply voltages for the switch drivers in each stage such that no additional voltage rail is required. Also, the bottom plate parasitic loss is lower, compared to single-stage 4:1 SC converters, which we further reduce via a charge recycling technique described below.

B. Bottom-Plate Charge Recycling

A dominant source of efficiency loss in SC converters comes from switching the bottom-plate parasitic capacitance associated with the flying capacitor (C_{FLY}). All of the flying capacitors in this design rely on bulk MOS transistors, which usually have non-negligible bottom-plate parasitic capacitance (~2% in this technology, ~5% in [4]). Each stage implements circuitry that combines two-step charging/discharging with charge recycling, as illustrated in Fig. 2 for the second stage. C_{PAR} is the parasitic bottom-plate capacitor of C_{FLY}. By adding an additional recycling capacitor, C_{REC}, the proposed technique avoids using an external voltage source. The two-step charging/discharging occurs during the converter's dead time to recycle charge, reduce losses, and improve conversion efficiency.

The charge recycling operation is as follows. Assume C_{REC}>>C_{PAR} and V_{REC} starts out at $V_{OUT}/2$. When discharging C_{PAR}, C_{PAR} first transfers charge to C_{REC} through the additional switch controlled by Φ_{REC}. In this process, C_{PAR} discharges from V_{OUT} to $V_{OUT}/2$. Then, the switch Φ_{REC} turns off and C_{PAR} fully discharges to gnd. The amount of charge transferred from C_{PAR} to C_{REC} is $C_{PAR}V_{OUT}/2$, which is stored on C_{REC} and is recycled in the charging phase. When charging C_{PAR}, C_{PAR} first charges up from gnd to $V_{OUT}/2$ via C_{REC}. In this period, C_{REC} transfers $Q=C_{PAR}V_{OUT}/2$ to C_{PAR}, which is the same amount of charge that C_{REC} gets from C_{PAR} in the discharging process. C_{PAR} then disconnects from C_{REC} and fully charges up to V_{OUT}. From an energy perspective, V_{OUT} only needs to provide $E=C_{PAR}V_{OUT}^2/2$ in this charging process, which is half of the energy otherwise required. It is important to note that V_{REC} eventually settles to $V_{OUT}/2$ regardless of its initial voltage, because this is the only balanced state where the energy stored on C_{REC} when discharging C_{PAR} matches the energy that C_{REC} loses when charging C_{PAR}.

The above recycling process assumes C_{REC}>>C_{PAR}. Thanks to the converter's multi-phase operation, C_{REC} can be shared by all of the phases and C_{REC} only needs to be larger than the parasitic capacitance in one phase, achieved with negligible penalty. In this implementation, C_{REC} is 2% of the total flying capacitance.

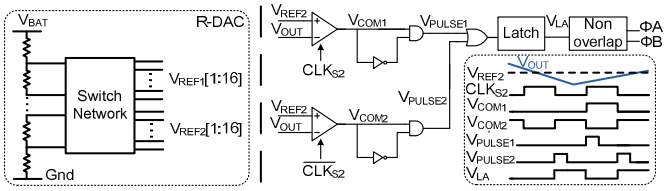


Fig. 3: Feedback control loop diagram (second stage)

C. Low-Boundary Feedback Control

Closed-loop operation regulates V_{OUT} and V_{INT} to desired voltage levels. Each stage implements the same low-boundary feedback control loop illustrated in Fig. 3 [3]. Since the feedback toplogy is the same in both stages, the following illustration uses the second stage as an example. Pairs of the interleaved modules share separate feedback paths, i.e., there are a total of eight feedback paths in the 2nd stage. In each feedback path, two comparators operate off of complimentary clocks generated by the VCO. The comparators compare V_{OUT} with a reference voltage, V_{REF2}, on the rising and falling edges of the clock. If V_{OUT} is smaller than V_{REF2}, V_{LA} switches either from low to high or high to low, depending on its previous state. V_{LA} then propagates through to control the power switches and switch the state of the SC converter. This action increases the output voltage V_{OUT}. If V_{OUT} is larger than V_{REF2}, V_{LA} remains in its previous state. The power swiches do not switch and V_{OUT} decreases until the SC converter reacts.

A resistor DAC (R-DAC), shown in Fig. 3, provides separate reference voltages to the 16 comparators via a switch network that connects each individual comparator to the resistor ladder separately. By doing do, we can use the R-DAC to calibrate comparator offsets. The switch network also generates 16 separate reference voltages for the first SC stage. Calibrating comparator offsets improves steady-stage voltage ripple and conversion efficiency.

III. Measurement Results

The two-stage SC converter was fabricated in TSMC's 40nm CMOS technology. The chip was tested in two modes: open- and closed-loop operation. In open-loop operation, the output voltage and output power can be tuned by changing the switching frequency , F_{sw}, of the converter via the VCO. In closed-loop operation, the VCO frequency is set to its maximum and the feedback control loop adjusts the effective switching frequency of the converter to regulate the output.

In open-loop operation, there is a relationship between the switching frequency and the output voltage and power. Shown in Fig. 4(a), higher output power requires high switching frequency to deliver energy more frequently. However, when switching frequency increases, there is less time for the switched capacitor circuit to settle in each cycle. Because of this incomplete charge transfer, the energy that is delivered from input to output in each cycle decreases as switching frequency increases. Hence, switching frequency increases super linearly with output power. Switching frequency, and thus switching loss, increases faster than the delivered power. Fig. 4(b) shows that higher output voltages also require higher switching frequencies. As the output voltage increases, there is less energy that can be delivered from input to output in each cycle [2]. So, switching frequency and switching loss increase faster than V_{OUT} increases.

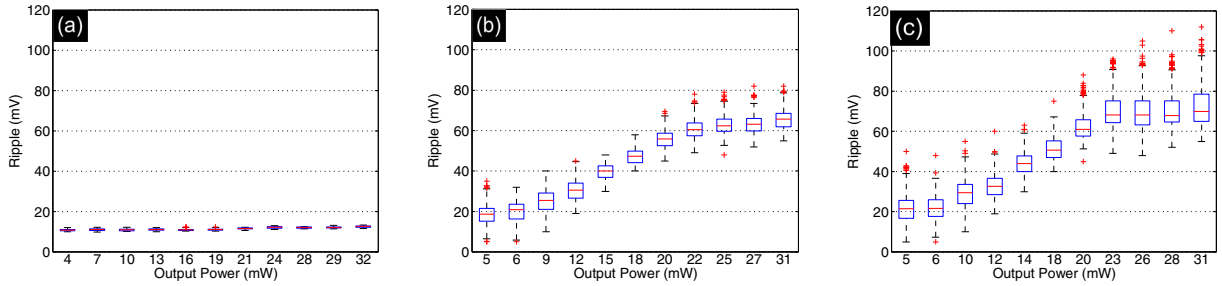


Fig. 5: Measured output voltage ripple @ V_{BAT}=3.8V, V_{OUT_AVE}= ~800mV in (a) open-loop operation, (b) closed-loop operation with calibrated comparators, and (c) closed-loop operation with un-calibrated comparators

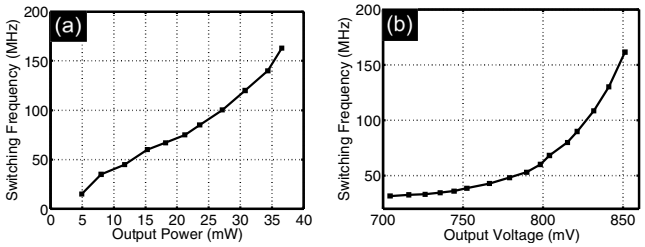
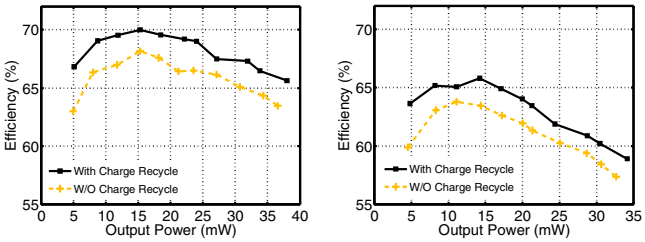
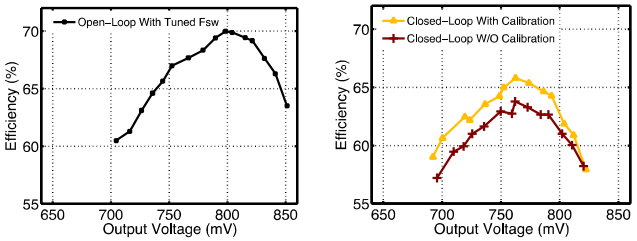


Fig. 4: Open-loop F_{sw} w/ V_{BAT}=3.8V for (a) different P_{OUT} @V_{OUT}=~800mV and (b) different V_{OUT} @I_{OUT}=~19mA



(a) open-loop operation (b) closed-loop operation

Fig. 6: Measured efficiency w/ V_{BAT}=3.8V & V_{OUT_MIN}=0.8V



(a) open-loop operation (b) closed-loop operation

Fig. 7: Measured efficiency w/ V_{BAT}=3.8V & I_{OUT}=~19mA

This section presents the experimentally measured results as follows: Section III.A first compares steady-state voltage ripple for open- and closed-loop modes of operation. Then, Section III.B presents conversion efficiency results versus V_{OUT} and P_{OUT}. The transient responses in open- and closed-loop modes of operation are discussed in Section III.C. Finally, Section D provides a summary of test chip characteristics and compares it to prior work.

A. Voltage ripple

The box plots in Fig. 5 compare the measured steady-state output voltage ripple across a range of output power conditions for the SC converter in open- and closed-loop operation. In open-lop operation, we manually tuned the VCO frequency to keep V_{OUT} at ~800mV for each power level. In closed-loop operation, the feedback loop keeps the output voltage at ~800mV. Steady-state ripple in open-loop operation is small (~10mV) due to the interleaved design with constant switching frequency. In contrast, closed-loop ripple is generally higher due to the cycle-skipping nature of the feedback topology. In each cycle, the feedback controller must determine whether the converter should switch or not. As a result, the instantaneous switching frequency can vary widely from cycle to cycle. Delay through the feedback loop further exacerbates the ripple, because the control loop must react to the output decreasing below the reference voltage. The longer the feedback delay is, the larger the ripple is. Measurement results show that closed-loop ripple increases with output power since larger load currents discharge the output voltage more quickly. Comparing Figs. 5(b) and (c), calibration helps to reduce voltage ripple by minimizing inconsistent switching thresholds across all of the comparators in the multiple feedback paths. In all subsequent plots, the comparators are always calibrated unless noted otherwise.

B. Conversion efficiency

In SC converters, the major sources of efficiency loss are due to linear charge redistribution loss, bottom-plate parasitic loss, other switching loss, and voltage ripple overhead. The minimum output voltage is used to calculate conversion efficiency, because the worst-case speed of the digital load circuits depends on the lowest transient voltage condition.

Fig. 6 plots efficiency measurements for both open- and closed-loop operation. In Fig. 6(a), open-loop efficiency reaches a peak of 70% at P_{OUT}=15mW. The efficiency rolls off for higher output power, because switching frequency and switching losses increase faster than the delivered power. Efficiency also rolls off for lower output power, because of static overheads. Comparing Figs. 6(a) and (b), closed-loop efficiency is generally lower than open-loop efficiency, because of larger voltage ripple. Fig. 6 also shows charge recycling consistently improves conversion efficiency by ~2%. Charge recycling is always on for all subsequent plots.

Fig. 7 plots conversion efficiency across different output voltage levels and exhibits the characteristic efficiency versus voltage curve of SC converters. In open-loop operation, the output voltage is set by tuning F_{SW}. In closed-loop operation, changing the reference voltage regulates the output voltage to different levels. Conversion efficiency rolls off as output voltage decreases due to linear charge redistribution loss and rolls off as output voltage increases due to higher switching loss.

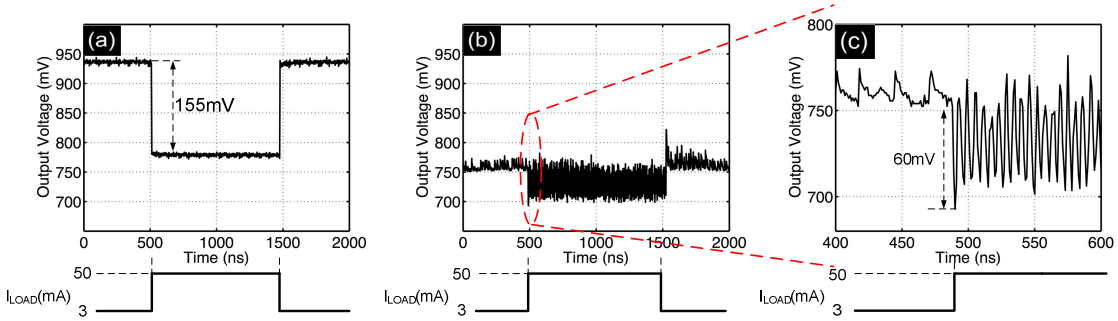


Fig. 9: Transient response (a) open-loop with maximum F_{SW}, (b) closed-loop, and (c) zoom-in of (b)

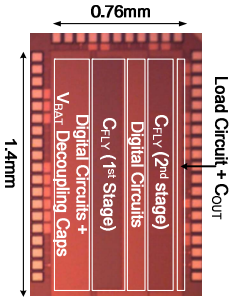
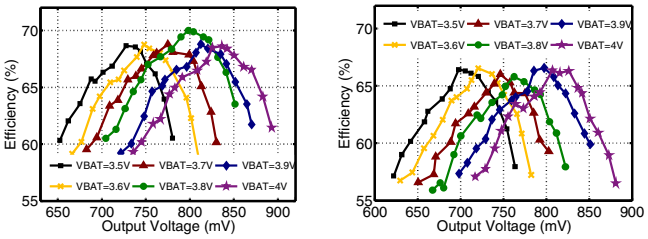


Fig. 10: Die Photo



(a) open-loop operation (b) closed-loop operation

Fig. 8: Measured efficiency with different V_{BAT} and V_{OUT_MIN}

Comparing the three curves in Fig. 7, open-loop operation consistently achieves higher conversion efficiency since it has the smallest voltage ripple. Calibration improves efficiency, as expected, since it reduces voltage ripple in closed-loop operation. The efficiency in closed-loop operation peaks at a lower output voltage compared with that in open-loop operation again because of voltage ripple and because the minimum output voltage is used to calculate efficiency.

Fig. 8 summarizes conversion efficiency versus output voltage for different battery voltages (V_{BAT}). First, conversion efficiency is higher for open-loop operation, consistent with previous results above. Second, conversion efficiency peaks at higher output voltages when V_{BAT} is higher since charge redistribution loss and switching loss are both related to V_{OUT}/V_{BAT} [2].

C. *Transient response*

Fig. 9 presents the SC converter's measured response to 47mA output load transients using an on-die load circuit with rise and fall times of ~100ps. As seen in Fig. 9(a), when the SC converter runs in open-loop with maximum switching frequency, a 3mA to 50mA load step causes V_{OUT} to drop by 155mV. When running in closed-loop with the nominal output voltage set to 750mV, however, the control loop quickly reacts and the voltage droop caused by the load current step is much smaller. In fact, the ~60mV droop in Fig. 9(c) is mostly due to the larger steady-stage voltage ripple previously seen with respect to higher output power.

D. *Test chip summary*

The silicon area, shown by the micrograph in Fig. 10, was not optimized for power density but was governed by the pads and circuitry added for testing. Flying capacitors and output filter capacitors, which occupy half of the overall area, total 2.64nF. Table. 1 compares this work to prior art SC converters. The 70% peak efficiency of this design is comparable to the efficiencies in [3] and [5], but for a higher 4:1 conversion ratio.

	[5]	[3]	This Work
Technology	65nm	90nm	40nm
Input voltage	3V-4V	3V-3.9V	3.5V-4V
C_{FLY}/C_{FILTER}	3.88nF/0	2nF/3.2nF	2.24nF/0.4nF
Efficiency (η) Peak eff. Conversion ratio	73% 74.3% 3:1	74% 77% 2:1	66% 70% 4:1
Power density (mW/nF)@η	31.3 (121mW/3.88nF)	28.8 (150mW/5.2nF)	13.3 (35mW/2.64nF)
Load step/C_{TOTAL} (mA/nF)@t_{rise}	41.7@50ps	5.8@25ns	17.8@100ps
Output droop	76mV	30mV	60mV

Table. 1 Comparison to prior art.

IV. Conclusions

This paper demonstrates a fully integrated battery-connected switched capacitor converter for the brain SoC of a microbotic bee. The two-stage topology, with bottom-plate charge recycling, offers high conversion efficiency for the high 4:1 conversion ratio. While closed-loop regulation provides fast transient response, it also exhibits larger stead-state voltage ripple, which results in efficiency drop compared to open-loop operation. This tradeoff motivates exploring an adaptive clocking strategy to improve overall system efficiency as described in [7].

Acknowledgments

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References

[1] M. Karpelson et al., Energetics of flapping-wing robotic insects: Towards autonomous hovering flight, *IROS*, 2010.

[2] H.-P. Le et al., Design techniques for fully Integrated switched-capacitor DC-DC converters, *JSSC*, Sep. 2011.

[3] T. Van Breussegem et al., Monolithic capacitive DC-DC converter with single boundary–multiphase control and…, *JSSC,* July 2011.

[4] Y.K. Ramadass et al., Voltage scalable switched capacitor DC-DC converter…, *PESC*, 2007.

[5] H.-P. Le et al., "A sub-ns response fully integrated battery-connected switched-capacitor voltage regulator…, *ISSCC,* 2013.

[6] W. Kim et al., A fully-integrated 3-level DC/DC converter for nanosecond-scale DVFS, *JSSC*, Jan. 2012.

[7] X. Zhang et al., Supply-noise resilient adaptive clocking for battery-powered aerial microrobotic system-on-chip in 40nm CMOS, submitted to *CICC*, 2013.

[8] T. Andersen et al., A 4.6 W/mm^2 power density 86% efficiency on-chip switched capacitor DC-DC converter in 32nm SOI CMOS, *APEC* 2013.