15.3 A Fully-Integrated 3-Level DC/DC Converter for Nanosecond-Scale DVS with Fast Shunt Regulation

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In recent years, chip multiprocessor architectures have emerged to scale performance while staying within tight power constraints. This trend motivates per-core/block dynamic voltage and frequency scaling (DVFS) with fast voltage transition. Given the high cost and bulk of off-chip DC/DC converters to implement multiple on-chip power domains, there has been a surge of interest in on-chip converters. This paper presents the design and experimental results of a fully integrated 3-level DC/DC converter [1] that merges characteristics of both inductor-based buck [2-4] and switched-capacitor (SC) converters [5]. While off-chip buck converters show high conversion efficiency, their on-chip counterparts suffer from loss due to low quality inductors. With the help of flying capacitors, the 3-level converter requires smaller inductors than the buck converter, reducing loss and on-die area overhead. Compared to SC converters that need more complex structures to regulate higher than half the input voltage, 3-level converters can efficiently regulate the output voltage across a wide range of levels and load currents. Measured results from a 130nm CMOS test-chip prototype demonstrate nanosecond-scale voltage transition times and peak conversion efficiency of 77%.

Shown in Fig. 15.3.1, the 3-level converter comprises a set of power FETs (P_{top}, PN_{mid}, N_{bottom}), a flying capacitor (C_{fly}), an inductor, and an output capacitor. The power FETs use thin-oxide devices with small parasitic resistance in a stacked structure to support input voltages (V_{in}) up to twice the maximum gate-source voltage allowed by the process technology. Level shifters generate input signals for P_{top} and PN_{mid}. This converter regulates the output voltage (V_{out}) by iterating through four steps per switching period (T). In steps 1 and 3, the converter relies on C_{fly}, whereas in steps 2 and 4, it relies on the inductor to regulate V_{out}. Duty cycle (D) sets the fraction of a switching period the converter operates in each step. When D equals 0.5 (50%), steps 2 and 4 essentially disappear and the converter operates like a SC converter, regulating the output to ~V_{in}/2. As D deviates away from 0.5, V_L swings between V_{in}/2 and V_{in} ($D > 0.5$), or 0 and V_{in}/2 ($D < 0.5$). The square-wave signal on V_L causes inductor current (I_L) ripple to vary with D and is filtered by the output inductor and capacitor to generate V_{out}. The 3-level converter offers advantages over conventional inductor-based converters that use large inductors [2,4] or high switching frequencies [3] to reduce I_L ripple, which otherwise causes large V_{out} ripple and increases resistive loss. Since the frequency of voltage swing on V_L is twice the converter's switching frequency, the converter can use lower switching frequencies and/or smaller inductors. Moreover, the amplitude of voltage swing on V_L is V_{in}/2, which further reduces I_L ripple and parasitic switching losses.

Figure 15.3.2 presents a block diagram of the test-chip prototype that comprises a pair of 2-phase, 3-level converters arranged as two identical sectors. To reduce ripple on V_{out}, the power FETs for each phase operate off of clock signals offset by 180 degrees. Low-impedance switches can connect the two sectors together to create a single 4-phase converter with each phase offset by 90 degrees. Otherwise, the test chip implements two independent 2-phase converters. An ability to disable power FETs also enables multiple 3-level converter configurations consisting of one to four phases. A programmable load in each sector facilitates experimental measurements by sinking up to 0.5A in 25mA steps as steady or pseudorandom patterns of current. The converter relies on a slow digital feedback loop to regulate V_{out} to a desired level by adjusting D. A supplemental shunt regulator suppresses output voltage fluctuations by detecting when V_{out} crosses low or high thresholds and injecting or extracting current to compensate for sudden load current fluctuations [6].

Data captured from a real-time oscilloscope (plotted in Fig. 15.3.3) demonstrates the converter can regulate the output voltage across a wide range—from 0.4 to 1.4V while operating off of a 2.4V input voltage—and rapidly scale V_{out} by 1V within 15 to 20ns. Such high-speed voltage transitions at nanosecond timescales enable complex digital systems to leverage temporally fine-grained DVFS and improve energy efficiency [7].

Figure 15.3.4 summarizes conversion efficiency measurements. The converter operates in open loop with fixed duty cycles ranging from 40% to 65% in 5% steps to facilitate measurements across a wide range of conditions. Two converter sectors can also operate with duty cycles that differ by 5% to implement finer steps. Since duty cycle is fixed during open-loop measurements, IR drop due to parasitic resistance causes a spread in output voltages with respect to load currents for the same duty cycle. Figure 4(a) aggregates all of the measured efficiencies collected across a range of static load current conditions (0.3 to 0.8A), duty cycles (40 to 65%), switching frequencies (50 to 160MHz), and number of phases (1 to 4). Efficiency peaks at 77% for low load current conditions at 50% duty cycle. Figure 15.3.4(b) compares measured data for 50% duty cycle operation using 2 and 4 phases. IR losses degrade efficiency as load current increases, worse for the 2-phase configuration. Higher switching frequency can also degrade efficiency at low load currents due to higher switching losses. Figure 15.3.4(c) plots the upper range of efficiency measurements for the 4-phase configuration by picking the best efficiency data across different duty cycle settings. Trend line overlays again illustrate the spread in output voltages due to IR drop. Since the 3-level converter merges characteristics of both SC and buck converters, efficiency peaks for 50% duty cycle. As duty cycle deviates from 50%, inductor current ripple grows and the corresponding increase in resistive losses degrades conversion efficiency. Figure 15.3.4(d) adds results for the 2-phase configuration (symbols with outlines) to show that fewer phases can sometimes improve efficiency at low load currents.

Figure 15.3.5 presents histogram plots of measured voltage noise, due to pseudorandom current patterns generated by the programmable loads, with and without the supplemental shunt regulator turned on. These results verify the shunt regulator can appreciably squeeze the noise distribution together and reduce peak-to-peak voltage excursions. Moreover, connecting the power domains reduces voltage noise as a result of larger output capacitance and some canceling of the pseudorandom load currents.

While the shunt regulator—reacting to threshold crossings—reduces voltage fluctuations, it has two drawbacks. First, internal circuit delays limit how quickly this feedback loop can sense and react. Second, simply relying on thresholds provides limited information as to the magnitude of voltage noise and the appropriate response needed to suppress it. One solution is to use a prediction-based shunt regulator that leverages microarchitecture-level information to reliably predict upcoming voltage droops [8]. Figure 15.3.6 presents snapshots of measured voltage droops due to two consecutive 80ns wide current pulses of 100mA and 150mA. Predictive current shunting reduces the maximum voltage droop by over 40% compared to simply reacting to threshold crossings.

Figure 15.3.7 presents a die micrograph and a list of specifications for the test chip.

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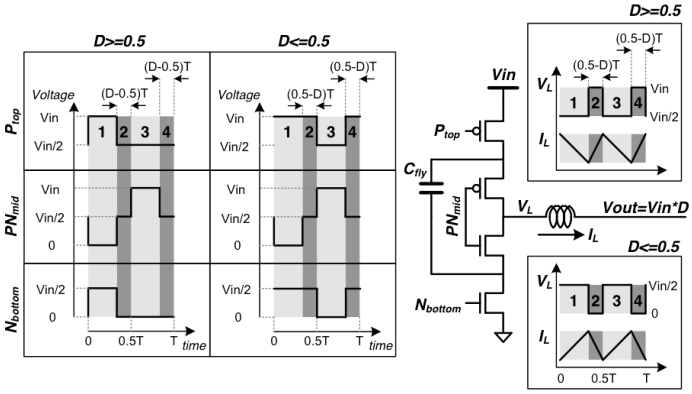

Figure 15.3.1: Schematic of the proposed 3-level power converter. Signal timing diagrams illustrate different operating modes.

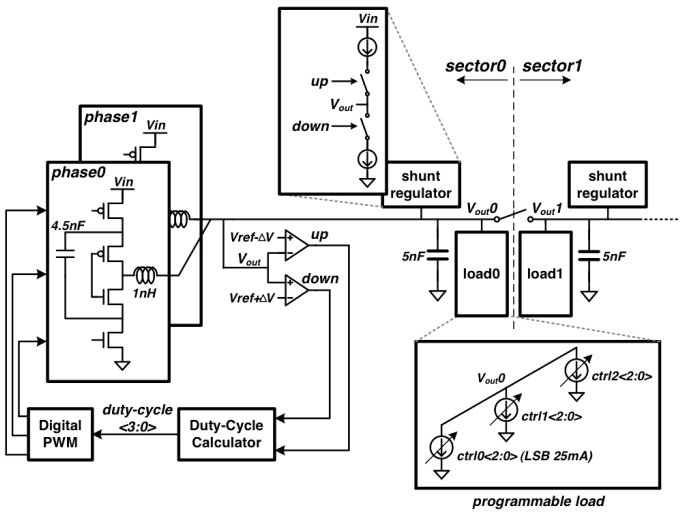

Figure 15.3.2: Block diagram of 3-level converter with slow digital feedback control and fast shunt regulation.

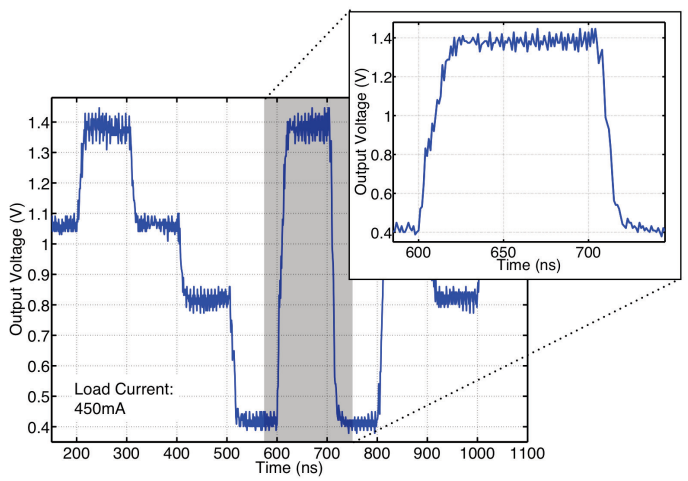

Figure 15.3.3: Measured snapshot of fast dynamic voltage scaling. Voltage scales from 1.4V to 0.4V and vice versa in 15-20ns.

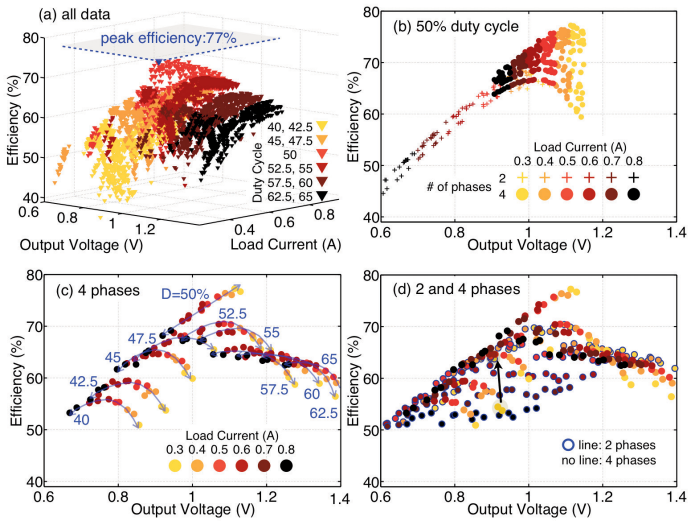

Figure 15.3.4: Measured conversion efficiency.

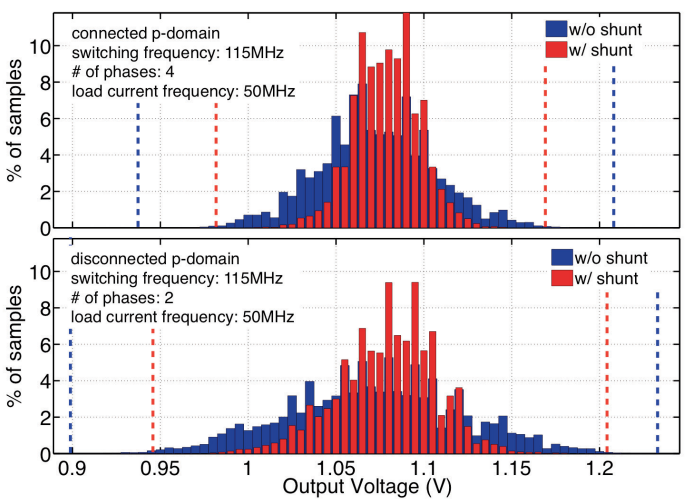

Figure 15.3.5: Histogram of measured voltage noise with and without shunt regulator for connected and disconnected power domains of two sectors.

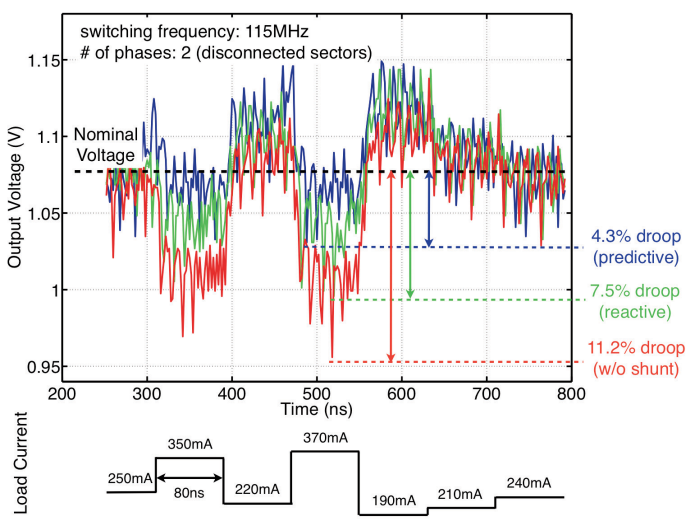

Figure 15.3.6: Comparison of measured on-die voltage noise without shunt regulator, with reactive shunt, and with predictive shunt.

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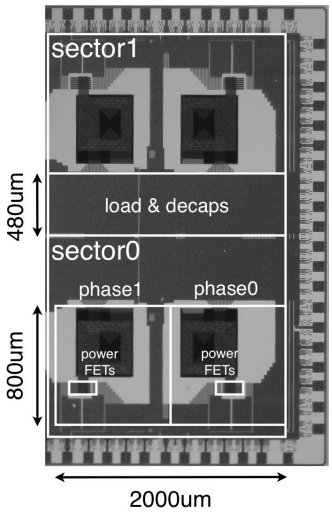

Technology	130nm CMOS
Load Power	0.2-1W
Input Voltage	2.4V
Output Voltage	0.4-1.4V
Inductor per phase	1nH
Total Flying Capacitance	18nF
Total Decoupling Capacitance	10nF
Switching Frequency	50-200MHz
Peak Efficiency	77%

Figure 15.3.7: Die micrograph of the converter with dimensions of main blocks. Flying capacitors with patterned ground planes sit under the inductors to save on-die area while maintaining inductor quality. The table shows converter specifications.

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