Design-Space Exploration of Backplane Receivers with High-Speed ADCs and Digital Equalization

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Abstract— **High-speed backplane receivers based on front-end ADCs with digital equalization facilitate design reuse, portability, and flexibility to reconfigure itself and accommodate different channel environments. However, power and complexity of such receivers can be high and require thorough high-level exploration to optimize design tradeoffs. This paper presents a backplane receiver model consisting of a simple, accurate, experimentally-verified, and parameterized high-speed flash ADC and a configurable digital equalizer for design-space exploration. Simulations demonstrate tradeoffs between ADC and equalizer bit resolution while maintaining constant receiver performance.**

I. Introduction

As data rates for backplane communications increase, high-speed transceivers require increasingly sophisticated equalization (EQ) to compensate for channel imperfections. This trend motivates using digital EQ with high-speed analog-to-digital converters (ADCs) at the front-end [1, 2]. Due to high data rates (>10Gbps), the front-end ADCs require high input bandwidth, but can tolerate low bit resolution [2, 3]. However, designing a low-power, high-speed ADC can be challenging and high-frequency digital EQ designs can be complex and high power. Given myriad tradeoffs one faces, this paper explores the design space of backplane receivers based on a simple-yet-accurate model of high-speed ADCs combined with a functional model of digital EQ. While the power and complexity implications remain as a future work, the proposed receiver model reveals the impact of different design parameters on performance. Simulation results show how one can trade between ADC and digital EQ resolution while maintaining constant receiver performance.

Receiver design-space exploration requires (1) an accurate model of high-speed ADCs and (2) a functional model of digital EQ. Section II presents a simple MATLAB model of a high-speed flash ADC that includes major non-ideal sources of error. Section III then verifies the model with experimental measurements from a test-chip prototype and explores the impact of different error sources. A combination of this ADC model and a functional model of digital EQ comprises the backplane receiver presented to facilitate thorough exploration of design tradeoffs in Section IV.

II. Behavioral Model of High-Speed ADC

One of the most important components of the proposed backplane receiver model is an accurate behavioral model of the high-speed ADC—simple to minimize simulation time and parameterized to understand tradeoffs. We assume a differential flash ADC architecture (shown Fig. 1) with a two-stage track-and-hold (TAH), based on a test-chip prototype presented in [3]. A two-stage TAH design supports high input data rates by relying on the second stage to buffer large loading, imposed by the comparators, from the high-bandwidth input stage. We further assume offset compensation in the comparator via a digital calibration loop that fine-tunes reference levels, also found in [3]. Hence, the proposed model consists of two major components: the two-stage TAH and multiple 1-bit comparators.

A. Two-stage TAH

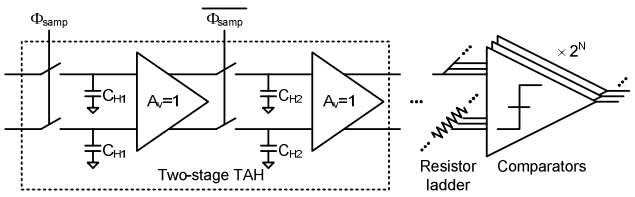


Fig. 1: An N-bit flash ADC architecture assumed in the model, based on [3].

CMOS TAH circuits have been carefully studied and found to suffer from several non-ideal error sources associated with the switches and buffers, listed in Table 1 [4, 5]. Although including all of these non-idealities would yield the most accurate ADC model, the correspondingly high complexity degrades simulation times. To keep the model simple, it only includes the dominant sources of error that noticeably affect ADC performance. For low-resolution ADCs, several sources are small enough to be masked by coarse-grained quantization and can be ignored. Moreover, several error sources can be corrected by simple cancellation circuits and digital calibration, as shown in [3]. Detailed simulations show that three random and signal-dependent error sources remain: sampling clock jitter, input-dependent sampling instant, and R_{on} variations. *Sampling clock jitter* adds random time offsets to ideal sampling instants, severely degrading ADC performance for high-frequency inputs. The *input-dependent sampling instant* error results from voltage-dependent MOSFET switching that perturbs the exact timing of when the switch turns off. Lastly, input-dependent fluctuations in "on" resistance of the switches (*R_{on} variation*) lead to bandwidth variations in the TAH. While this effect is comparatively small, it noticeably degrades ADC performance, especially when combined with the input-dependent sampling instant error.

Switch		Unity gain buffer	
Sampling clock jitter	✓	Gain error	Corr.
Input-dependent sampling instant	✓	Nonlinearity	Corr.
R_{on} variation	✓	Offset	Corr.
Clock feedthrough	Small		
Input feedthrough	Small		
Pedestal	Corr.		
Droop	Small		

Table 1: Sources of TAH error [4, 5].

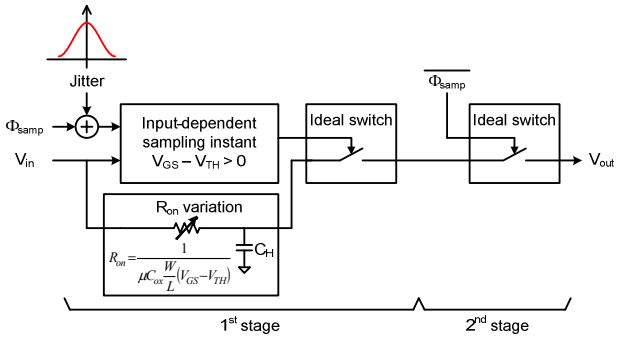


Fig. 2: Model of non-ideal two-stage TAH.

Fig. 2 illustrates the resulting non-ideal model of the two-stage TAH, implemented in MATLAB. Since the TAH converts the continuous-time input signal (V_{in}) into a discrete-time output (V_{out}), simulations are run in two phases. For high accuracy, the two-stage TAH model uses fine time steps (t_{step}=t_{pd_clk}/2000) and relies on shape-preserving cubic interpolation to further increase resolution (t_{fine}=t_{step}/100) around important time intervals (i.e. clock edges) while avoiding large simulation times. The remainder of the ADC model (and digital EQ) simulates in discrete time and can be fast. Clock jitter, modeled as Gaussian noise, adds random time offsets to an ideal clock edge (Φ_{samp}) with parameterized rise time and generated with t_{fine} steps. To model the input-dependent sampling instant error, the shifted clock edge is compared to a cubic-interpolated input signal to determine when V_{GS}–V_{TH} = (V_{clk}–V_{in})–V_{TH} = 0, which corresponds to the actual sampling instant. An RC low-pass filter models the R_{on} variation before capturing the sampled voltage with an ideal switch. Since the second TAH stage tracks a settled output it can be modeled as an ideal switch.

B. Comparator

The one-bit comparators that follow the two-stage TAH also suffer from non-idealities that require careful modeling. As shown in Fig. 3, the comparator model includes two major components of error—offset and meta-stability. While we assume offset compensation via digital calibration, finite resolution of offset correction resolution results in residual comparator offset that cannot be ignored. This residual offset adds a uniformly-distributed random voltage, with bounds defined by the limited resolution of offset correction, to the ideal reference voltage level (V_{ref_ideal}). While an ideal comparator can resolve arbitrarily small input differences, noise governs how a real comparator resolves. Hence, the reference voltage includes an additional Gaussian-distributed random offset (μ=0, σ=0.1% of ADC supply voltage).

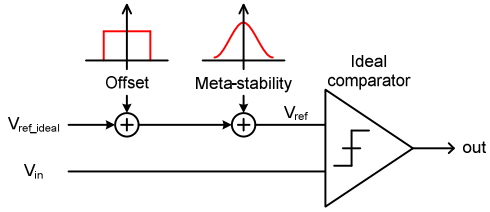
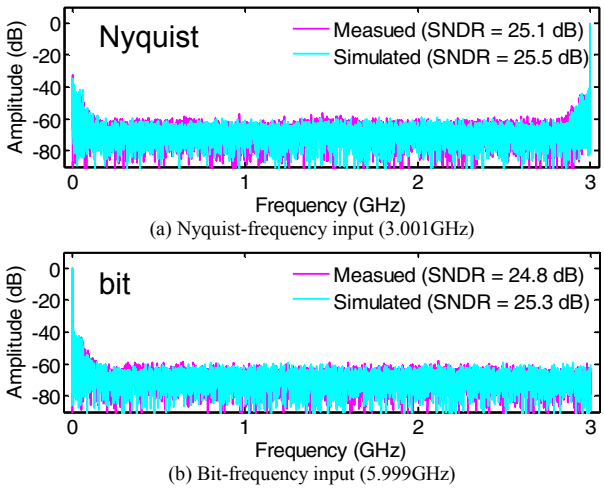


Fig. 3: Model of non-ideal 1-bit comparator



(a) Nyquist-frequency input (3.001GHz)

(b) Bit-frequency input (5.999GHz)

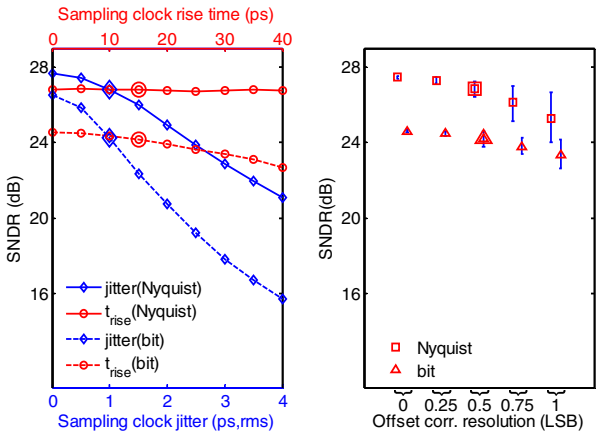
Fig. 4: Comparison of measured and simulated FFT plots at 6-GS/s.

III. Verification and Analysis of ADC Model

In order to use the proposed ADC model to explore design-space tradeoffs in the receiver, it is important to first verify its accuracy and investigate the impact of the non-ideal error sources in the model.

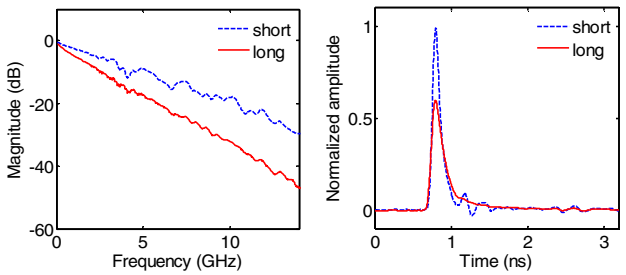
Fig. 4 compares the simulated output FFT of the ADC model operating at 6-GS/s with both Nyquist- and bit-frequency inputs to experimental measurements from the test-chip prototype in [3]. Various model parameters, such as sampling clock jitter, rise time, and comparator offsets, were chosen based on measurement results. The simulation setup includes a front-end auto-gain controller (AGC) to match the experimental setup, but is not in the final ADC model. Since high-speed ADCs are often interleaved to further enhance data rates (discussed in Section IV), a comparison of measured and simulated output FFTs with a bit-frequency sine wave input is also shown. The overlays of FFT plots and SNDR numbers reveal good agreement between simulated and measured results, which verifies the model's ability to accurately emulate high-speed ADC behavior.

This experimentally-verified model offers early-stage investigations to establish targets for critical specifications that dictate design effort and govern ADC performance. For example, design of PLLs and buffers affect clock jitter; buffer sizing affects clock edge rates and power; and minimum resolution for offset compensation affects complexity of the digital calibration circuitry. For this analysis, we assume a 4.5-bit ADC operating at 6.25-GS/s. Fig. 5 plots the simulated SNDR, again with both Nyquist- and bit-frequency inputs, across a range of values for clock jitter, clock rise time, and offset correction resolution with baseline values of 1-ps-rms, 15-ps, and 0.5-LSB, respectively. Fig. 5(a) shows that clock jitter has the most significant impact on ADC performance, and the effects of clock edge rates are small. Fig. 5(b) plots the average and peak-to-peak SNDR for 100 sets of simulations with random uniformly-distributed offsets. While ADC performance improves with finer offset correction, the overall impact is small compared to the effects of clock jitter.



(a) Sampling clock (b) Residual comparator offset

Fig. 5. Effect of design parameters on ADC performance: (a) Sampling clock jitter and rise time (b) Residual comparator offset



(a) Frequency response (b) Pulse response at 12.5-Gbps

Fig. 7: Backplane channel model characteristics.

IV. Backplane Receiver with Digital Equalization

Building upon the ADC model, we now construct the entire MATLAB model of the backplane transceiver, illustrated in Fig. 6, to explore receiver design tradeoffs. A transmitter adds 1-ps of rms jitter to the data symbols driven onto the band-limited backplane channel. Our analysis considers two backplane channel models—short (1-inch) and long (20-inches) copper traces on FR4 with connectors, provided by Intel and available at [7]. Fig. 7 plots their respective frequency and pulse responses. An ideal AGC scales the received signal to the full input range of the ADC. A pair of half-rate ADCs generates two sets of outputs that are time-interleaved into a single full-rate, N-bit symbol stream. The subsequent M-bit digital EQ block consists of j-tap feed-forward equalization (FFE) followed by k-tap decision feedback equalization (DFE) with loop unrolling. The two channels require different amounts of equalization, leading to a 1-tap FFE + 5-tap DFE and 2-tap FFE + 8-tap DFE used for the short and long channels, respectively. Sign-error LMS and sign-sign LMS algorithms adaptively update FFE and DFE tap weights, respectively.

Since this model is intended for preliminary design-space exploration, digital EQ blocks are simple functional models and do not yet include detailed power and delay limitations imposed by real designs. For example, final designs would parallelize the FFE and DFE blocks to alleviate speed bottlenecks and simplify digital multiplication (in the FFE) to minimize complexity [1, 6].

Given the challenges associated with high-speed ADC and symbol-rate adder designs required for digital EQ, we explore the impact of varying the bit-level resolutions of the N-bit ADC and M-bit digital EQ on receiver performance, represented by the mean-square error (MSE) of the equalizer, normalized to the desired received-symbol amplitude. Using bit-error rate (BER) as the comparison metric leads to prohibitively long simulation times. Fig. 8 presents simulation results of the full transceiver model operating at 12.5-Gb/s for both short and long channels across a range of ADC and digital EQ resolutions. These results assume aforementioned baseline values for ADC non-idealities. Clearly, maximizing both N and M minimizes error, but comes at high costs in terms of power and complexity. The surface plots reveal a range of N- and M-bit resolutions that offer constant receiver performance with equal MSE (lines shown for 0.004 MSE). For the short channel, one can reduce ADC resolution by 1.5 bits at the expense of increasing resolution in the digital EQ by 6 bits to compensate for the coarse-grained quantization of the received symbols. This model works towards a way to eventually scale ADC and digital EQ resolution depending on their relative power/performance vs. number of bits.

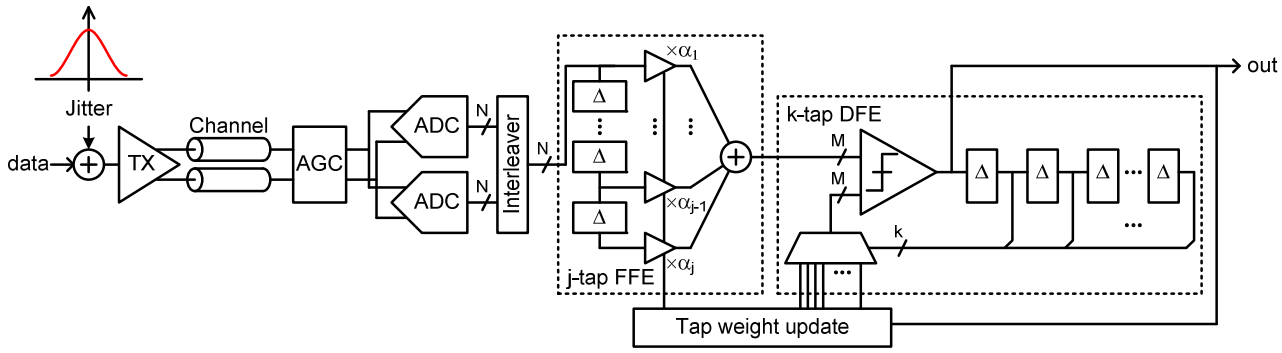
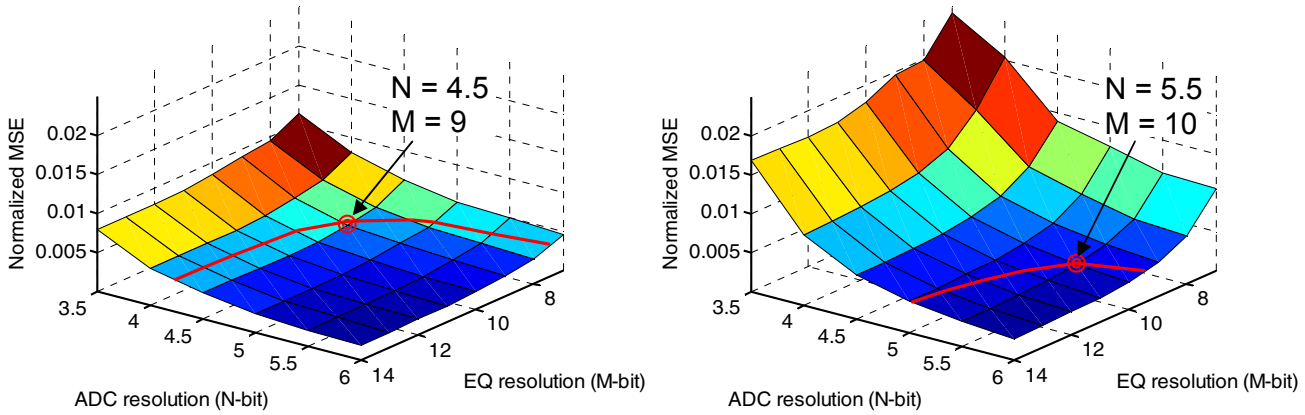
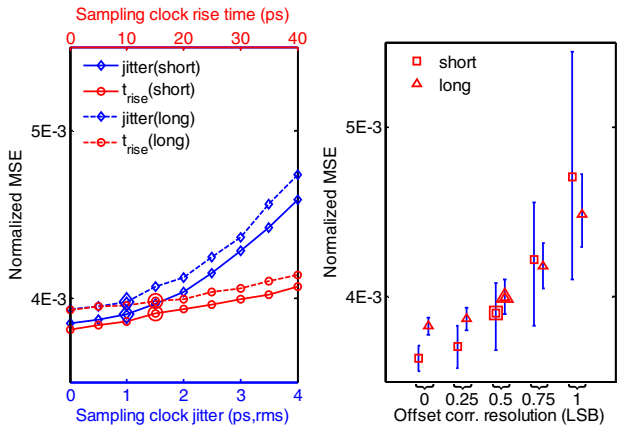


Fig. 6: Full high-speed backplane transceiver model with ADC front-end receiver and adaptive digital EQ.



(a) Short channel (b) Long channel

Fig. 8: Normalized MSE vs. ADC and EQ resolution for short and long channels.



(a) Sampling clock (b) Residual comparator offset

Fig. 9: Effects of ADC design parameters on receiver performance.

To further explore the receiver's design space, we choose the closest points to the 0.004 MSE line (identified by the circles) that minimize both N and M on the two surface plots of Fig. 8. Fig. 9 compares the effects of clock jitter, clock edge rise time, and resolution of offset error correction (i.e. residual error), again possible with the parameterized ADC model, for these design points. These simulations again assume the same set of baseline values as before (identified by the big symbols) in the ADC-only analysis and show interesting trends. While clock jitter is the clearly dominant error source that degrades SNDR in the ADC, residual offsets in the ADC also play a significant role in affecting the resulting MSE for the overall receiver. On average, efforts to improve offset correction by 0.25 LSB offer larger gains in receiver performance than it does to eliminate clock jitter. Extensive investigations of such relationships and tradeoffs allow the designer to efficiently allocate design effort during the early phase of design.

VI. Conclusion

This paper demonstrates design-space exploration of backplane receivers relying on a simple-yet-accurate model of a high-speed flash ADC and a functional model of digital EQ. The ADC model has been verified by comparing simulation results to experimental results from a test-chip prototype, as it is perhaps the most critical and challenging component to model accurately. While simulation-based investigations of only the ADC motivate designers to prioritize design efforts to minimize clock jitter, simulations of the overall receiver model reveal opportunities to improve performance by reducing residual offsets in the comparators. Broad design-space sweeps of ADC and digital EQ resolution provide guidelines on trading off resolution between the two while maintaining constant performance.

This paper has focused primarily on developing the simple-yet-accurate model for the high-speed ADC. By combining it with a functional model of digital EQ, we have shown its utility for preliminary design-space explorations. Future work seeks to augment these models with circuit-level power, delay, and design complexity relationships and limitations, to enable thorough exploration of related costs and identify optimum design points.

Acknowledgments

We would like to thank the Mixed-Signal Communications IC Design Group at IBM T. J. Watson Research Center for their support of this work.

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