Design Considerations for ADC-Based Backplane Receivers

(Invited Paper)

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***Abstract*— High-speed ADC-based backplane receivers often suffer from high power consumption and complexity and require careful designs. This paper discusses circuit- and system-level design considerations for such receivers. A low-power, high-speed front-end ADC circuit and a high-level design-space exploration of ADC-based receivers are presented.**

I. Introduction

As demands for high data rates increase, high-speed backplane receivers require more and more equalization to compensate for channel imperfections. In recent years, backplane receivers that rely on front-end analog-to-digital converters (ADCs) followed by digital equalizers have been widely investigated [1]–[10] to fully exploit benefits of advanced digital signal processing (DSP) techniques. However, designing such ADC-based receivers is non-trivial; both front-end ADCs and digital equalizers suffer from high power consumption and complexity when data rate is high. Therefore, careful circuit design and system-level optimization are required in order to meet tight power and performance budgets of backplane transceivers.

This paper presents circuit- and system-level design techniques for ADC-based receivers. Section II discusses circuit techniques for a low-power, high-speed front-end ADC design. A two-stage track-and-hold amplifier (THA) with duty cycle control enables high sampling rates with low power consumption. Section III, then, presents system-level optimization of ADC-based receivers. A high-level model of an ADC-based receiver allows fast and through design-space exploration.

II. Front-end ADC design

Designing front-end ADCs for backplane receivers is challenging because they require high input bandwidths and sampling rates to deal with high-speed (i.e. 10's of Gbps) signals, while the power consumption should be kept low to meet tight power budgets of backplane receivers. Since high-speed ADCs often consume high power due to high-bandwidth THAs and high degree of time interleaving [11], [12], power consumption of the front-end ADCs is one of the major concerns in ADC-based receiver design. Luckily coarse ADC resolution (i.e. 4–6 bit) is acceptable as digital equalizers can deal with it.

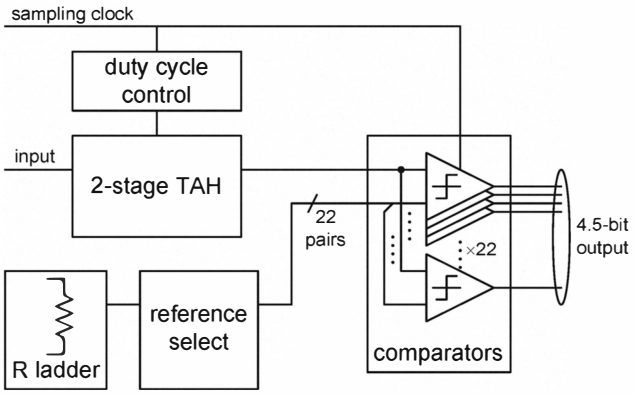

Fig. 1. A 4.5-bit flash-type front-end ADC architecture [13]

A front-end ADC with a two-stage THA and duty cycle control has been presented [13] to achieve high-speed and low-power operation at the same time. Fig 1 shows the overall architecture of the 4.5-bit front-end ADC. A flash-type structure is adopted for high sampling rate. However, large capacitive loading on the THA output due to 22 parallel comparators can limit the THA input bandwidth. Therefore, a two-stage THA [14] is employed.

Fig. 2 shows circuit and timing diagrams of the two-stage THA. Each THA stage consists of small PMOS switches, dummy switches for charge injection cancellation and differential amplifiers. Switches in each stage are driven by complementary clocks. The cross-coupled capacitors in differential amplifiers help reduce glitches on the THA outputs. The two-stage THA separates the input node, that requires high bandwidth to deal with high-speed signals, from the heavily loaded output. Since the second stage tracts a settled voltage held by the first stage, low bandwidth can be accepted in the second stage to save power.

To aggressively push sampling rate, duty cycle of the sampling clock is extended to allow more tracking times at the heavily-loaded second stage when the sampling rate is high. Widening the duty cycle from 50% to 58% effectively increases sampling rates by 14%.

This two-stage THA structure with duty cycle control sig-

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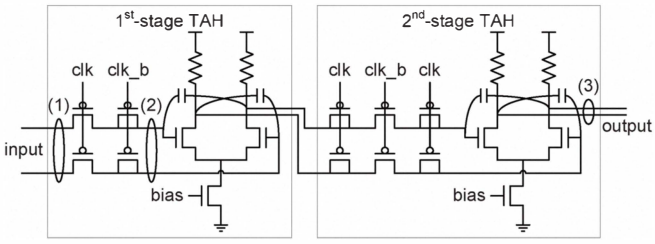
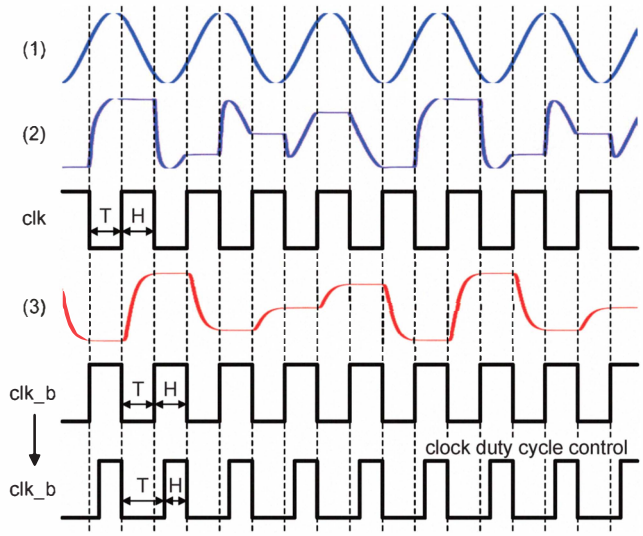
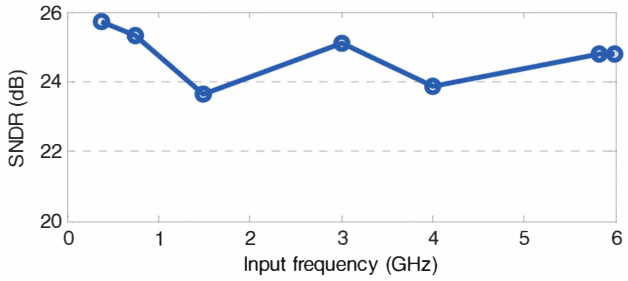


(a) THA Circuit

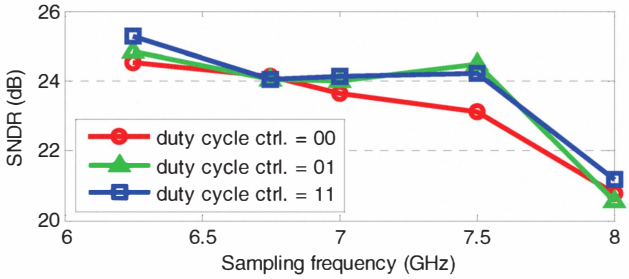


(b) Timing diagram and duty cycle control

Fig. 2. Two-stage THA with duty cycle control [13]



(a) SNDR vs. input frequency at 6-GS/s



(b) SNDR vs. sampling frequency (with Nyquist input frequencies)

Fig. 3. Measured ADC performance [13]

nificantly reduces the ADC power consumption and improves input bandwidth and sampling rate. Fig. 3 plots the signal-to-noise and distortion ratio (SNDR) measured from a test chip prototype fabricated in 65-nm CMOS. Fig. 3(a) shows that the ADC has high input bandwidth, while Fig. 3(b) demonstrates that the duty cycle control can improve SNDR to 24.5dB at 7.5-GS/s. The overall ADC power consumption is only 52-mW at 7.5-GS/s and the resulting figure-of-merit (FOM) is 0.5-pJ/conversion-step.

III. Receiver Design-Space Exploration

One of the main challenges in ADC-based receiver design is meeting tight power and performance budgets of backplane transceivers. Since both front-end ADCs and digital equalizers can be power consuming and complex at high data rates, a system-level design optimization based on a thorough design-space exploration is crucial to meet the tight power and performance budgets.

Receiver design-space exploration requires a parameterized high-level model of a receiver that can accurately estimate receiver performance within a short period of time. To enable fast and accurate simulations, we constructed a high-level model of an ADC-based receiver in MATLAB [4]. Fig. 4 illustrates the transceiver architecture assumed for the receiver design-space exploration. The receiver consists of two time-interleaved front-end ADCs and an adaptive digital equalizer that comprises a feed-forward equalizer (FFE) and a decision feedback equalizer (DFE). Simple functional models can be used to estimate a digital equalizer performance as digital circuits are immune to noise and process variations. On the other hand, front-end ADCs require an accurate behavioral model as they deal with high-speed analog signals. At the same time, the model should be simple enough to enable fast simulations. Therefore, a simple-yet-accurate behavioral model of front-end ADC, verified with experimental results from at test chip prototype, has been presented [4].

Utilizing the high-level model, wide ranges of design parameters—such as ADC resolution, equalizer resolution and number of equalizer taps—can be swept to explore the design-space of ADC-based receivers [4]. Fig. 5 shows an example of design-space exploration. We swept the front-end ADC and digital equalizer resolutions to investigate design-space of a 12.5-Gps receiver over a long (i.e., 20-inch) backplane channel provided by Intel [15]. The surface plot reveals a range of ADC and equalizer resolutions that offer constant receiver performance with equal mean-square error (MSE). The design points with 0.004 MSE (shown in a red line) suggest that one can reduce ADC resolution by 1 bit at the expense of increasing resolution in the digital equalizer by 4 bits to compensate for the coarse-grained quantization of the received symbols. Eventually, such results provides a guideline to scale ADC and equalizer resolutions depending on their relative power/performance vs. number of bits.

The design-space exploration can also provide guidelines for front-end ADC design [4]. Fig. 6 illustrates the effect of ADC design parameters (i.e., sampling clock jitter, rise time and comparator offset correction resolution) on ADC

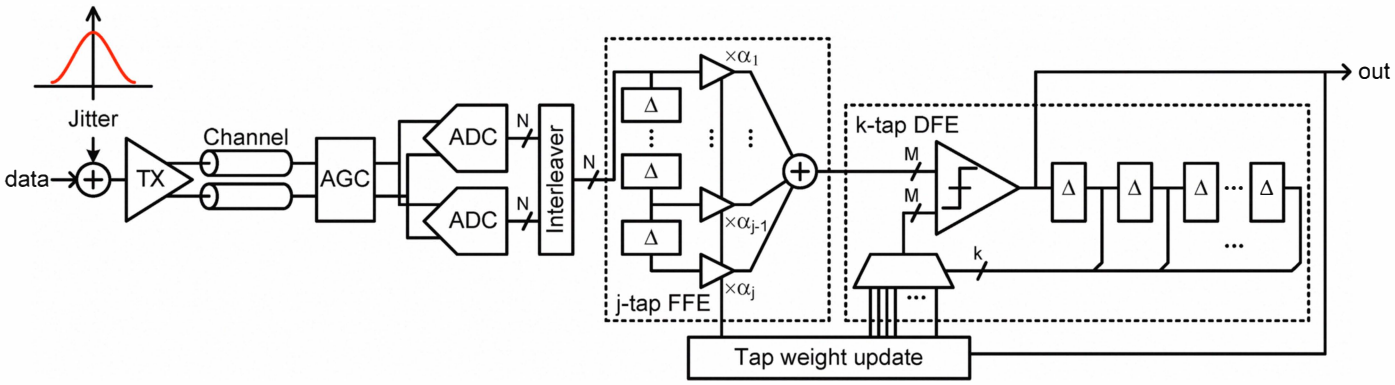


Fig. 4. High-speed backplane transceiver model assumed for ADC-based receiver design-space exploration [4]

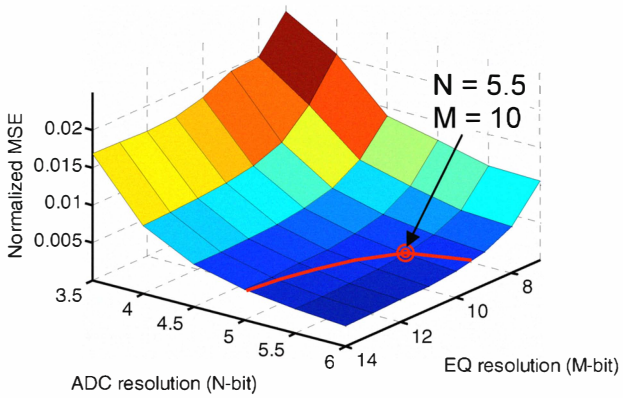


Fig. 5. Design-space exploration: normalized MSE vs. ADC and equalizer resolutions [4]

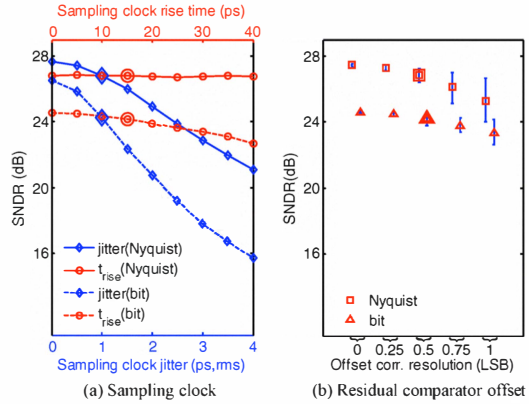


Fig. 6. Effect of design parameters on ADC performance: (a) sampling clock jitter and rise time and (b) residual comparator offset [4]

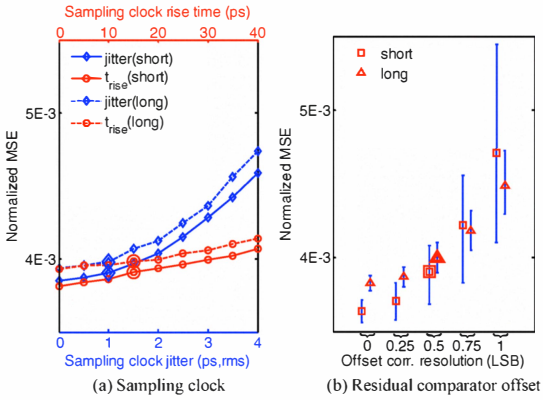


Fig. 7. Effect of ADC design parameters on receiver performance: (a) sampling clock jitter and rise time and (b) residual comparator offset [4]

performance. We assumed a 4.5-bit ADC operating at 6.25-GS/s and used SNDR as a performance measure. The plot shows that sampling clock jitter has the most significant impact on ADC performance and the effects of sampling clock rise time and comparator offset correction resolution are relatively small.

While the sampling clock jitter clearly is the key design parameter for the ADC-only performance, it may change when the overall ADC-based receiver performance is concerned. Fig. 7 shows the effect of ADC design parameters on overall receiver performance. Notice that, comparator offset correction resolution plays the most significant role in receiver performance. On average, improving offset correction resolution by 0.25 LSB offers larger gains in receiver performance than it does to eliminate clock jitter. Extensive investigations of such tradeoffs between design parameters allow the designer to efficiently allocate design efforts during the early stage of design.

IV. Conclusion

This paper discusses circuit- and system-level design considerations for ADC-based backplane receivers. As high power consumption of front-end ADCs is one of the main concerns in ADC-based receivers, circuit techniques for a low-power high-speed ADC are presented. A two-stage THA with sampling clock duty cycle control enables 0.5-pJ/conversion-step at 7.5-GS/s. Then, system-level design optimization techniques, that are crucial to meet tight power and performance budgets, are discussed. A thorough design-space exploration reveals that one can trade ADC bits with digital equalizer bits depending on their relative power/performance vs. number of bits. Also, further parameter sweeps demonstrate that comparator offset

correction resolution is the most significant ADC design parameter when the overall receiver performance is concerned, while sampling clock jitter affect the ADC-only performance the most.

ACKNOWLEDGMENT

We would like to thank the Mixed-Signal Communications IC Design Group at IBM T. J. Watson Research Center for their support of this work.

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