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Design of CMOS Adaptive-Bandwidth PLL/DLLs: A General Approach

Jaeha Kim, *Member, IEEE*, Mark A. Horowitz, *Fellow, IEEE*, and Gu-Yeon Wei, *Member, IEEE*

***Abstract*—A phase-locked loop (PLL) and delay-locked loop (DLL) design with adaptively adjusting bandwidth enables optimal performance over a wide frequency range and across process, voltage, and temperature variations. A design methodology of such adaptive-bandwidth PLLs and DLLs is described. To assess the impact of each circuit parameter directly, we derive a discrete-time, open-loop dynamic model of the PLL/DLL that characterizes the change in output variables in response to the sampled error and we express the adaptive-bandwidth criteria in terms of the open-loop gains, instead of the traditional closed-loop parameters, ω_n and ζ. Applying these criteria, we derive scaling equations for the charge-pump current and filter resistance that achieve adaptive bandwidth in charge-pump PLL/DLLs. We show that previously published adaptive-bandwidth PLL/DLLs, a self-biased PLL/DLL and a regulated-supply PLL/DLL, rely on the small-signal conductance tracking the large-signal conductance of the voltage-controlled oscillator/voltage-controlled delay-line and, thus, sustain constant $\omega_n/\omega_{\rm ref}$ and ζ only if the voltage swing is sufficiently higher than the device threshold voltage $V_{\rm TH}$. The paper also presents procedures to estimate the open-loop parameters from an open-loop impulse response of the PLL/DLL.**

***Index Terms*—Adaptive bandwidth, delay-locked loop (DLL), phase-locked loop (PLL).**

I. Introduction

ADAPTIVE-BANDWIDTH phase-locked loops (PLLs) and delay-locked loops (DLLs) refer to a class of PLLs and DLLs that scale their loop dynamics proportionally with the reference frequency [1], [2]. For example, in a linear PLL [4], an adaptive-bandwidth PLL maintains a constant ratio between the loop bandwidth and the reference frequency and keeps the damping factor constant regardless of process, temperature, and voltage variation. Various circuit techniques to realize adaptive bandwidth have been published [1]–[3]. This paper tries to find a common underlying design principle in those different circuit techniques and to provide a guideline for those who wish to design an adaptive-bandwidth PLL or DLL in a sub100-nm CMOS technology.

An adaptive bandwidth that tracks with the operating frequency helps sustain the best jitter performance of the PLL or DLL over a wide frequency range. A PLL or DLL is inherently a sampled-data system, in which the loop bandwidth must be at least a decade below the reference frequency in order to avoid instability due to the sampling delay. In a fixed-bandwidth PLL, the bandwidth is thus constrained to be a decade below the lowest desired operating frequency, as depicted in Fig. 1. Therefore, at frequencies other than this minimum, the PLL has a bandwidth lower than its possible maximum. Since the bandwidth determines a loop's response rate to reject self-induced noise, e.g., voltage-controlled oscillator (VCO) noise, it means that the PLL has suboptimal performance in the upper frequency range. On the other hand, in an adaptive-bandwidth PLL, the bandwidth scales with the operating frequency and maintains optimal performance of the PLL for all frequencies.

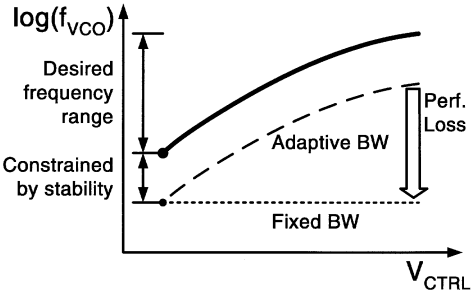

Fig. 1. Adaptive bandwidth versus fixed bandwidth in case of a wide frequency range. The fixed bandwidth results in performance loss in most of the range.

The adaptive bandwidth helps achieve the best performance even when the target frequency range is narrow. Variations in process, voltage, and temperature can lead to uncertainties in loop parameters such as VCO gain, charge-pump current, and feedforward zero frequency. These uncertainties force a designer to choose a conservative operating point that guarantees stable operation for all conditions, which is unfortunately not the best-performance point in most cases. Fig. 2(a) illustrates the case with a typical CMOS ring oscillator. Variations in process, voltage, and temperature cause the VCO frequency to vary by a factor of $2 \sim 3$ between its slowest and fastest conditions. Therefore, the oscillator must have a wide enough tuning range to ensure operation at the target frequency, even if the target frequency is just a single point. Fig. 2(b) plots the variation in loop bandwidth due to variation in VCO gain, which is derived from the slope of the VCO tuning curves in Fig. 2(a). To ensure stability, the designer must select the bandwidth based on the worst-case condition—in this case, the fastest corner—resulting in suboptimal bandwidths for all other cases. In other words, the design margins to cope with uncertainties reduce the best jitter performance achievable. As we shall see, an adaptive-bandwidth PLL adapts the charge-pump current and loop-filter (LF) resistance to the VCO's operating

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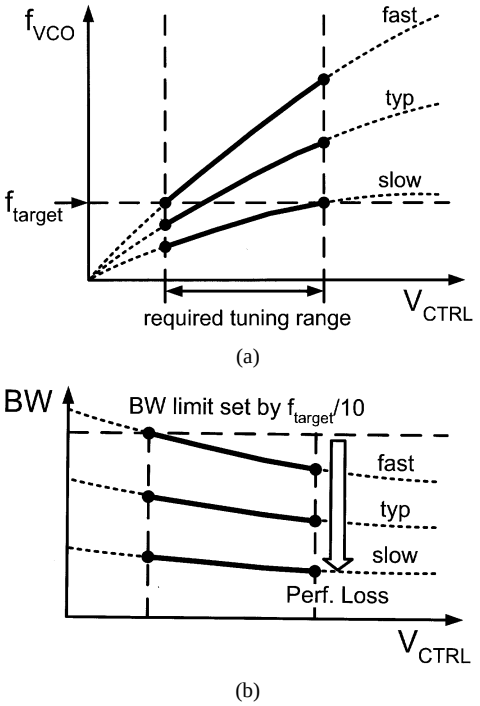

Fig. 2. (a) Variation in VCO frequency. (b) Variation in VCO gain due to process, voltage, and temperature (PVT) variations. Design margins to ensure stability against uncertainties cause performance loss.

condition, so that the variation in VCO gain is effectively compensated. Since the expected bandwidth then falls into a narrower range, the designer can reduce margin and design for higher bandwidth operation.

This paper derives the criteria for adaptive-bandwidth PLL/DLLs and examines the implementations published in literature based on these criteria. The most popular way of describing a PLL or DLL is to use closed-loop parameters such as bandwidth ω_n and damping factor ζ. Despite their direct implication on the loop's frequency response and stability, PLL circuit designers often find it cumbersome to translate closed-loop criteria into open-loop criteria. For example, it is challenging to find the scaling requirement for the charge-pump current or the LF resistance to maintain adaptive-bandwidth operation over a wide frequency range. Thus, Section II introduces a new dynamical model for a PLL/DLL that focuses on the open-loop transfer function between the phase error and the resulting change in output variables, rather than the closed-loop transfer function between the input and output phases. The adaptive-bandwidth criteria are then expressed in open-loop parameters, C_ϕ and C_ω.

Section III applies these new criteria to the charge pump PLL/DLL and derives the requirements for scaling the charge-pump current and the LF resistance to satisfy the conditions necessary for adaptive-bandwidth operation. Section IV then discusses the common design principles used in the self-biased PLL [1] and the regulated-supply PLL [2], each of which implements adaptive bandwidth using different circuit techniques. The analysis reveals that their design principles are in fact approximations to the exact requirements and meet the criteria only in the large-swing regime. We will discuss their limitations as a wider frequency range is pursued or as the nominal supply voltage drops in future generations of CMOS technology. Section V comments on the methods to estimate the open-loop parameters from the time-domain transients obtained from simulation or measurement.

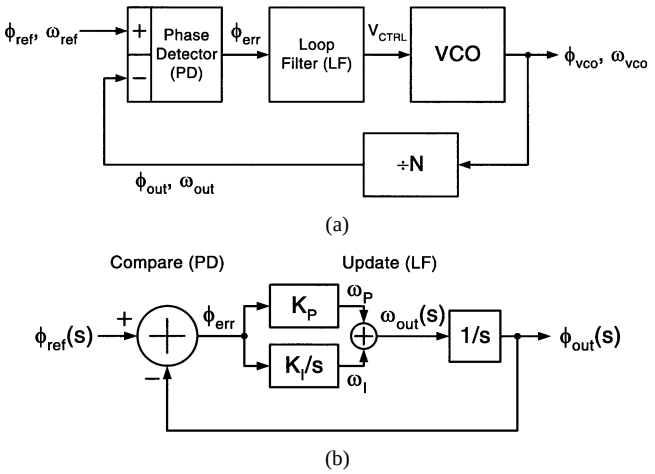

Fig. 3. (a) Block diagram. (b) Continuous-time model of a second-order linear PLL.

II. Discrete-Time Open-Loop Criteria of Adaptive-Bandwidth PLL/DLLs

Fig. 3(a) is a block diagram of a second-order linear PLL [4]. A PLL is a feedback system that tries to match the VCO output phase $\phi_{\rm out}$ and frequency $\omega_{\rm out}$ to those of the reference clock, $\phi_{\rm ref}$ and $\omega_{\rm ref}$, respectively. In case of frequency multiplication, the outputs $\phi_{\rm out}$ and $\omega_{\rm out}$ are some fractions $(1/N)$ of the VCOs direct outputs $\phi_{\rm vco}$ and $\omega_{\rm vco}$. Thus, when $\phi_{\rm out}$ is locked to $\phi_{\rm ref}$, $\phi_{\rm vco}$ is equal to $N\phi_{\rm ref}$ and the frequency is multiplied. While $\phi_{\rm vco}$ and $\omega_{\rm vco}$ are of more practical interest, we will instead use $\phi_{\rm out}$ and $\omega_{\rm out}$ as the output variables in the analysis. As we will see, the use of $\phi_{\rm out}$ and $\omega_{\rm out}$ eliminates the explicit notation of the multiplication factor N and keeps the analysis simple. If desired, $\phi_{\rm vco}$ and $\omega_{\rm vco}$ can be easily calculated as $N\phi_{\rm out}$ and $N\omega_{\rm vco}$, respectively.

A variety of PLL implementations exists, ranging from analog implementations to fully digital ones [7], [8], but most linear PLLs with orders higher than two have the following control dynamics. A phase detector (PD) measures the error between the two phases, $\phi_{\rm ref}$ and $\phi_{\rm out}$. Upon the detection of the phase error, $\phi_{\rm err}$, a LF makes appropriate adjustments on the VCO frequency $\omega_{\rm out}$ to reduce this error. First, the LF typically employs an integral control, which sets the VCO base frequency ω_I to a time-integral of the past phase error scaled by a gain K_I. The integral control helps suppress static phase offset because it ensures that the loop will not settle until $\phi_{\rm err}$ reaches zero. However, the integral control can make the feedback unstable since it results in two poles placed at dc, where the second pole comes from the time-integration of the frequency to a phase via the VCO. To stabilize this feedback loop, the LF also needs a compensating zero or a proportional control, which adds another term ω_P, as shown in Fig. 3(b). The frequency ω_P is set proportional to the current phase error. The sum of ω_I and ω_P constitutes the VCO frequency $\omega_{\rm out}$. PLLs with orders higher than two may have additional poles

and/or zeros in their LFs to gain extra control over subcycle behaviors, for instance, frequency spurs [11], [13]. However, since those high-order poles/zeros are placed well beyond the loop bandwidth to ensure stability, they have little effect on determining the loop bandwidth. The second-order analysis provided here should suffice to derive the necessary criteria for adaptive-bandwidth operation.

The natural frequency ω_n and the damping factor ζ are derived from the closed-loop transfer function of the PLL [14]. Note that the integral and the proportional gains, denoted as K_I and K_P in Fig. 3(b), are the total gains around the loop, including the gains of the phase detector, the LF, the VCO, and also the dividing ratio $1/N$. First, the open-loop transfer function of the PLL, $G_{\rm PLL}(s)$, defined as $\phi_{\rm out}(s)/\phi_{\rm err}(s)$, is

$$\begin{aligned} G_{\rm PLL}(s) &= \frac{\phi_{\rm out}(s)}{\phi_{\rm err}(s)} \\ &= \frac{sK_P + K_I}{s^2}. \end{aligned} \tag{1}$$

Then, the closed-loop transfer function $H_{\rm PLL}(s) = \phi_{\rm out}(s)/\phi_{\rm ref}(s)$ is

$$\begin{aligned} H_{\rm PLL}(s) &= \frac{G_{\rm PLL}(s)}{1 + G_{\rm PLL}(s)} \\ &= \frac{sK_P + K_I}{s^2 + sK_P + K_I} \\ &\equiv \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \end{aligned} \tag{2}$$

From the definition shown in the last line of (2), we can express ω_n and ζ in terms of K_P and K_I

$$\begin{aligned} \omega_n &= \sqrt{K_I} \\ \zeta &= \frac{K_P}{2\omega_n} = \frac{K_P}{2\sqrt{K_I}}. \end{aligned} \tag{3}$$

An adaptive-bandwidth PLL requires that $\omega_n/\omega_{\rm ref}$ and ζ are held constant over the desired range of $\omega_{\rm ref}$. Equation (3) then implies that the open-loop gains K_I and K_P must satisfy the relations, $K_I = \omega_n^2 \propto \omega_{\rm ref}^2$ and $K_P = 2\zeta\omega_n \propto \omega_{\rm ref}$, respectively. Although these conditions are sufficient to design an adaptive-bandwidth PLL, we will carry out a little more analysis to find an intuitive meaning of this open-loop form of the adaptive-bandwidth criteria.

The open-loop transfer function $G_{\rm PLL}(s)$ in (1) characterizes the relationship between the phase error $\phi_{\rm err}$ and the output phase $\phi_{\rm out}$. Although $\phi_{\rm err}$ was described as a continuous-time quantity in Fig. 3(b), it is in fact a discrete-time sampled value. For binary clock waveforms, since the phase detector can detect a timing error only by comparing the clock edge positions, the phase comparison can occur only once per cycle. Therefore, the PLL is essentially a discrete-time system that acts upon the sampled phase error every reference cycle.

From this point of view, we can redescribe the open-loop transfer function of the PLL in a discrete-time domain, as shown in Fig. 4. The integral control $\omega_I(s) = K_I\phi_{\rm err}(s)/s$ can be regarded as a discrete-time summation

$$\omega_I[n] = \omega_I(nT_{\rm ref}) = \sum_{i=-\infty}^{n-1} K_I \cdot T_{\rm ref} \cdot \phi_{\rm err}(iT_{\rm ref}) \tag{4}$$

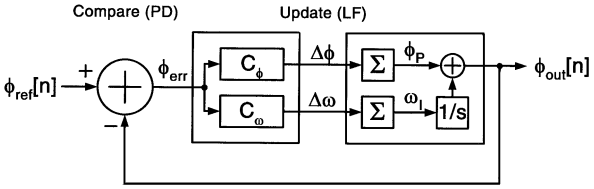

Fig. 4. A discrete-time PLL modeling the changes in phase $\Delta\phi$ and in frequency $\Delta\omega$ of each cycle due to the sampled phase error $\phi_{\rm err}$.

where $T_{\rm ref}$ is the reference cycle time, $2\pi/\omega_{\rm ref}$. Similarly, the proportional control $\omega_P(s) = K_P\phi_{\rm err}(s)$ can also be regarded as a discrete-time summation if the resulting phase $\phi_P(s) = \omega_P(s)/s$ is considered as the output

$$\phi_P[n] = \phi_P(nT_{\rm ref}) = \sum_{i=-\infty}^{n-1} K_P \cdot T_{\rm ref} \cdot \phi_{\rm err}(iT_{\rm ref}). \tag{5}$$

An alternative view is that in each cycle the LF updates the frequency ω_I and phase ϕ_P by quantities that are proportional to the current sampled error $\phi_{\rm err}$

$$\begin{aligned} \Delta\omega &= \omega_I[n] - \omega_I[n-1] \\ &= K_I \cdot T_{\rm ref} \cdot \phi_{\rm err} = \frac{2\pi K_I}{\omega_{\rm ref}} \cdot \phi_{\rm err} \\ \Delta\phi &= \phi_P[n] - \phi_P[n-1] \\ &= K_P \cdot T_{\rm ref} \cdot \phi_{\rm err} = \frac{2\pi K_P}{\omega_{\rm ref}} \cdot \phi_{\rm err}. \end{aligned} \tag{6}$$

Then ω_I and ϕ_P are the sums of the past $\Delta\omega[n]$'s and $\Delta\phi[n]$'s, respectively. The output phase $\phi_{\rm out}$ is the sum of ϕ_P and the time-integral of ω_I, $\phi_I(s) = \omega_I(s)/s$.

Equation (6) is an open-loop dynamic equation that models the change in phase and frequency due to each sampled phase error. Since $K_I = \omega_n^2$ and $K_P = 2\zeta\omega_n$, (6) becomes

$$\begin{aligned} \Delta\omega &= 2\pi\omega_{\rm ref}\left(\frac{\omega_n}{\omega_{\rm ref}}\right)^2 \cdot \phi_{\rm err} \\ \Delta\phi &= 4\pi\zeta\frac{\omega_n}{\omega_{\rm ref}} \cdot \phi_{\rm err}. \end{aligned} \tag{7}$$

Therefore, this equation and the adaptive-bandwidth criteria, i.e., the constant $\omega_n/\omega_{\rm ref}$ ratio and damping factor ζ, imply that the relative change in frequency $\Delta\omega/\omega_{\rm ref}$ and the change in phase $\Delta\phi$ of an adaptive-bandwidth PLL are equivalent to the phase error $\phi_{\rm err}$ scaled by some constant values. By denoting these constants as C_ω and C_ϕ, respectively, we get the open-loop dynamic equation of the adaptive-bandwidth PLL as below

$$\begin{aligned} \frac{\Delta\omega}{\omega_{\rm ref}} &= C_\omega \cdot \phi_{\rm err} \\ \Delta\phi &= C_\phi \cdot \phi_{\rm err} \end{aligned} \tag{8}$$

where C_ω is defined as $2\pi(\omega_n/\omega_{\rm ref})^2$ and C_ϕ as $4\pi\zeta(\omega_n/\omega_{\rm ref})$.

This new form of adaptive bandwidth criteria, i.e., constant open-loop gains, C_ω and C_ϕ, implies that instead of estimating ω_n and ζ from the closed-loop frequency response, one can verify an adaptive-bandwidth PLL by measuring the changes in the output phase and frequency made upon a unit phase error. Although these open-loop gains were derived from a second-order analysis, their definitions can also be extended to higher-

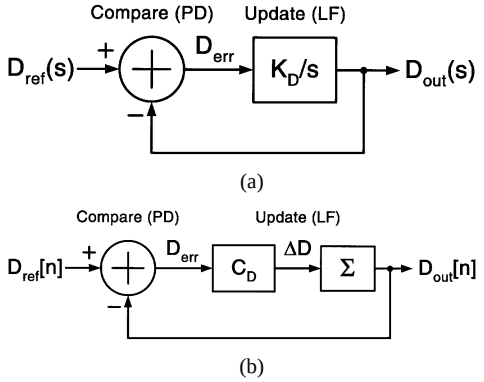

Fig. 5. DLL dynamic models. (a) Continuous-time model. (b) Discrete-time model characterizing ΔD of each cycle.

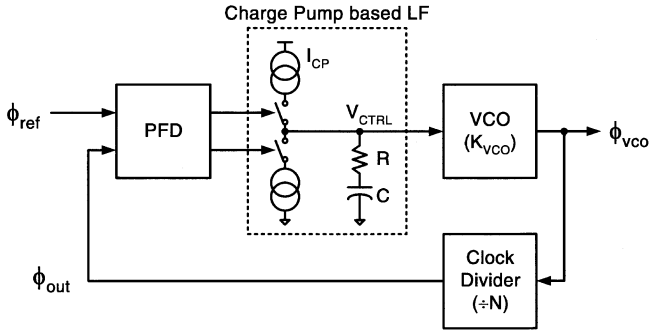

Fig. 6. A charge-pump PLL. The main parameters that must vary to keep adaptive bandwidth are I_{cp} and R.

order PLLs and used to evaluate their bandwidths. The methodology for estimating C_ω and C_ϕ from the open-loop response and the case with higher order PLLs will be described in Section V. As will be seen in Section III, this open-loop dynamic equation of (8) also provides better intuition to optimize the circuit parameters and helps derive the exact scaling requirements for those circuit parameters that achieve adaptive bandwidth over the desired frequency range of operation.

It is handy to remember the formulas that convert the open-loop parameters back to the closed-loop parameters: $\omega_n/\omega_{\rm ref} = \sqrt{C_\omega/2\pi}$ and $\zeta = C_\phi/\sqrt{8\pi C_\omega}$. For instance, C_ω of 0.02 and C_ϕ of 0.7 corresponds to $\omega_n/\omega_{\rm ref}$ of 0.056 and ζ of 0.99, a design target of most wide-bandwidth PLLs.

We can derive similar criteria for adaptive-bandwidth DLLs. A DLL modeled in Fig. 5(a) locks the delay of a voltage-controlled delay-line (VCDL) $D_{\rm out}$ to a desired delay $D_{\rm ref}$. The main difference from a PLL is that the VCDL does not involve an integration. Therefore, the feedback loop is stable with only an integral control that suppresses static delay offset. The resulting system is then a first-order system with only one state variable, $D_{\rm out}$.

Let us first find the bandwidth ω_n from the continuous-time DLL model shown in Fig. 5(a). With integral control alone, $D_{\rm out}$ is equal to a gain K_D times the time-integral of the past delay error, $D_{\rm err} = D_{\rm ref} - D_{\rm out}$. As in the PLL analysis, this gain K_D encompasses the gain contributions from the phase detector, LF, and VCDL. The closed-loop transfer function of the DLL, $H_{\rm DLL}(s)$ is then

$$H_{\rm DLL}(s) = \frac{D_{\rm out}(s)}{D_{\rm ref}(s)} = \frac{K_D}{s+K_D} \equiv \frac{\omega_n}{s+\omega_n}. \tag{9}$$

From (9), we find that $\omega_n = K_D$. For a DLL to satisfy the adaptive-bandwidth criteria, i.e., constant $\omega_n/\omega_{\rm ref}$ ratio, the loop gain K_D must scale proportionally with reference frequency $\omega_{\rm ref}$.

Like a PLL, a DLL is also a discrete-time system since its phase detector can measure the delay difference only once every cycle. Therefore, we can derive a discrete-time open-loop transfer function similar to (8). The integral control is converted to a discrete-time summation of $K_D \cdot T_{\rm ref} \cdot D_{\rm err}(nT_{\rm ref})$ and the change in $D_{\rm out}$ due to each sampled delay error is

$$\begin{aligned}\Delta D &= D_{\rm out}[n] - D_{\rm out}[n-1] \\ &= K_D \cdot T_{\rm ref} \cdot D_{\rm err} = \frac{2\pi K_D}{\omega_{\rm ref}} \cdot D_{\rm err} \\ &= 2\pi \frac{\omega_n}{\omega_{\rm ref}} \cdot D_{\rm err}. \end{aligned} \tag{10}$$

Therefore, the adaptive-bandwidth criterion of constant $\omega_n/\omega_{\rm ref}$ implies that the gain C_D in the following open-loop dynamic equation must be constant

$$\Delta D = C_D \cdot D_{\rm err} \tag{11}$$

where C_D is equal to $2\pi\omega_n/\omega_{\rm ref}$. At each cycle, the output delay is adjusted by ΔD which is equal to the sampled delay error $D_{\rm err}$ scaled by C_D. A C_D of 0.5 corresponds to a $\omega_n/\omega_{\rm ref}$ ratio of 0.08.

III. Adaptive-Bandwidth Charge-Pump PLL/DLLs

Section II derived the adaptive-bandwidth criteria expressed in open-loop gains: constant C_ϕ and C_ω for PLL and constant C_D for DLL. This section applies these criteria to charge-pump PLLs and DLLs, one of the most popular forms of PLL/DLL implementations today. For the case of charge-pump PLLs, the main parameters that determine the open-loop gains are the charge-pump current I_{cp} and filter resistance R. A job of an adaptive-bandwidth PLL designer is therefore to select proper values for I_{cp} and R, and to design circuits that scale these parameters with respect to $\omega_{\rm ref}$. This section derives the scaling requirements for I_{cp} and R of adaptive-bandwidth PLL/DLLs and Section IV will discuss how these scalings can be realized with CMOS circuits.

A block diagram of a charge-pump PLL is shown in Fig. 6 [5]. The LF consists of a charge pump followed by a passive *RC* filter. The phase-frequency detector generates pulses whose widths are proportional to the phase error and the charge pump dumps either positive or negative charge onto a capacitor (C) for the duration of those pulses. While inactive, the charge pump has infinite output impedance, which enables a robust realization of pure integration (the pole located at dc). Therefore, the

loop gain at dc is ideally infinite and the gain-related static offsets are eliminated.[1] The resistance (R) in series with the capacitor implements the proportional control (the zero). During the charge transfer, the transient current through the resistor results in a voltage whose aggregate effect over a full period is proportional to the present phase error.

To apply the open-loop adaptive-bandwidth criteria in (8), the change in frequency $\Delta\omega$ and that in phase $\Delta\phi$ are first calculated

$$\begin{aligned}\Delta\omega &= \frac{K_{\rm VCO}}{N}\cdot\frac{I_{cp}}{C}\cdot T_{\rm err}\\ &= \frac{K_{\rm VCO}}{N}\cdot\frac{I_{cp}}{C}\cdot\frac{\phi_{\rm err}}{\omega_{\rm ref}} \qquad (12)\\ \Delta\phi &= \frac{K_{\rm VCO}}{N}\cdot I_{cp}R\cdot T_{\rm err}\\ &= \frac{K_{\rm VCO}}{N}\cdot I_{cp}R\cdot\frac{\phi_{\rm err}}{\omega_{\rm ref}} \qquad (13)\end{aligned}$$

where I_{cp} is the charge-pump current, R is the LF resistance, C is the LF capacitance, $K_{\rm VCO}$ is the VCO gain (in rad/s/V), and N is the dividing ratio of the clock divider. Since adaptive-bandwidth operation requires the two open-loop gains $C_\omega = \Delta\omega/\omega_{\rm ref}/\phi_{\rm err}$ and $C_\phi = \Delta\phi/\phi_{\rm err}$ be constant, we get the following scaling requirements on I_{cp} and R as the reference frequency $\omega_{\rm ref}$ varies.

First, from (12) and constant C_ω, the charge-pump current I_{cp} must satisfy

$$\begin{aligned}\frac{1}{I_{cp}} &= \frac{1}{C_\omega\cdot C}\cdot\frac{\frac{K_{\rm VCO}}{N}}{\omega_{\rm ref}^2}\\ &\propto \frac{1}{\omega_{\rm ref}^2}\cdot\frac{1}{N}\frac{\partial\omega_{\rm vco}}{\partial V_{\rm CTRL}}\\ &= \frac{1}{\omega_{\rm ref}^2}\cdot\frac{\partial\omega_{\rm ref}}{\partial V_{\rm CTRL}}\\ &= -\frac{\partial}{\partial V_{\rm CTRL}}\left(\frac{1}{\omega_{\rm ref}}\right)\\ &\propto -\frac{\partial T_{\rm ref}}{\partial V_{\rm CTRL}} \qquad (14)\end{aligned}$$

assuming that the loop capacitance C is held at a fixed value. In other words, $I_{cp}\propto -\partial V_{\rm CTRL}/\partial T_{\rm ref}$ and the charge-pump current must scale with the rate of change of the final $V_{\rm CTRL}$ for a unit change in the reference cycle. Second, by applying (13) and (14), and constant C_ϕ, the scaling requirement on the filter resistance R is obtained

$$\begin{aligned}R &= \frac{C_\phi\cdot\omega_{\rm ref}}{\frac{I_{cp}\cdot K_{\rm VCO}}{N}}\\ &= \frac{C_\phi}{C_\omega\cdot C}\cdot\frac{1}{\omega_{\rm ref}}\\ &\propto T_{\rm ref}. \qquad (15)\end{aligned}$$

The filter resistance R must vary proportional to the reference cycle. Equations (14) and (15) are, therefore, the key requirements for an adaptive-bandwidth charge-pump PLL.

A charge-pump DLL has a similar configuration to a PLL shown in Fig. 6, except that the LF does not have a series resistor. Every cycle, the phase detector generates a pulse whose width is equal to the delay error and the charge pump either charges or discharges a capacitor C while the pulse is asserted. Changes on the voltage across the capacitor $V_{\rm CTRL}$ then result in the adjustment of the VCDL delay. The change in delay ΔD due to a delay error $D_{\rm err}$ is calculated

$$\Delta D = K_{\rm VCDL}\cdot\frac{I_{cp}}{C}\cdot D_{\rm err}. \qquad (16)$$

where $K_{\rm VCDL}$ is the VCDL gain defined as $-\partial D_{\rm out}/\partial V_{\rm CTRL}$.[2] Then, the constant $C_D = \Delta D/D_{\rm err}$ required for an adaptive-bandwidth DLL implies that the charge-pump current I_{cp} must satisfy

$$\begin{aligned}\frac{1}{I_{cp}} &= \frac{1}{C_D\cdot C}\cdot K_{\rm VCDL}\\ &\propto -\frac{\partial D_{\rm out}}{\partial V_{\rm CTRL}}. \qquad (17)\end{aligned}$$

This criterion (17) is in fact an identical criterion to (14), especially if the PLL and the DLL use the same buffer stages for their VCO and VCDL, respectively. The circuit techniques to scale the charge-pump current for an adaptive-bandwidth PLL can thus be applied directly to an adaptive-bandwidth DLL.

IV. CMOS Implementation Examples

Section IV-A and IV-B visit two CMOS adaptive-bandwidth PLLs published in the literature: a self-biased PLL with symmetric-load buffers [1] and a regulated-supply PLL with CMOS inverters [2]. Both designs rely on scaling the charge-pump current as the control voltage $V_{\rm CTRL}$ to compensate for changes with VCO gain. Equations (14) and (15) will help us understand why these designs work and what can be a challenge as we stretch these designs to next-generation CMOS processes. We will find that the assumptions that these designs are based on break down as the voltage swing in the buffer gets closer to the device threshold voltage $V_{\rm TH}$. Therefore, the operating range that satisfies adaptive bandwidth will shrink as the nominal supply of the CMOS process continues to scale down relative to $V_{\rm TH}$; some ways to get around these limits are suggested. Discussions focus mainly on the design of the adaptive-bandwidth PLLs, since the criterion (17) for the adaptive-bandwidth DLL is identical to that of the PLL in (14).

A. Self-Biased PLLs With Symmetric-Load Buffers

Fig. 7 presents the VCO of the self-biased PLL proposed in [1]. Each buffer is a differential stage with a so-called symmetric load, which is a parallel combination of a diode-connected pMOS device and a near-triode pMOS device with its gate connected to $V_{\rm SWING}$. Within the output voltage range between V_{DD} and $V_{\rm SWING}$, the symmetric load exhibits symmetric I–V characteristics and thus a nearly constant output resistance, $R_{\rm sym}$, averaged throughout the swing. This attribute enables the buffer to reject high-frequency noise by equalizing the rising and falling output transitions and, thus, reduces jitter [9].

A replica-feedback biasing circuit in Fig. 7 dynamically controls the voltage swing and the bias current of the oscillator.

[1]The main causes of the remaining static offsets in charge-pump PLLs are the mismatch between the up and down currents of the charge pump, the mismatch within the phase-frequency detector, and the mismatch between the reference clock path and the feedback clock path.

[2]The negative sign is from the assumption that the delay $D_{\rm out}$ decreases as $V_{\rm CTRL}$ increases, for being consistent with the VCO case where the frequency $\omega_{\rm out}$ increases as $V_{\rm CTRL}$ increases.

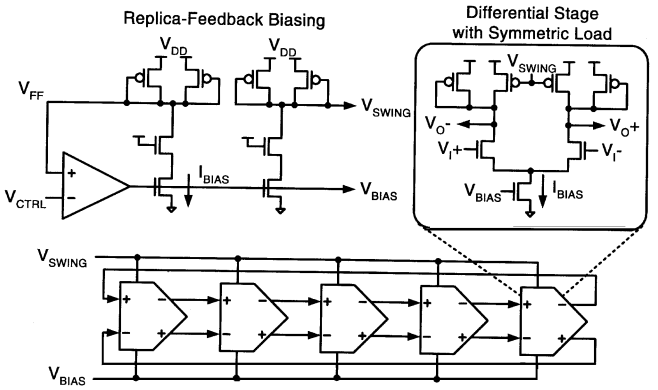

Fig. 7. The VCO and the replica-feedback biasing circuit of the self-biased PLL.

A feedback amplifier adjusts the bias current $I_{\rm BIAS}$ so that the voltage drop across the symmetric load, i.e., the voltage swing of the VCO buffers, is equal to $V_{DD} - V_{\rm CTRL}$. A half-buffer replica in the bias generator translates $I_{\rm BIAS}$ to $V_{\rm SWING}$ through a diode-connected device, whose output resistance mimics that of the symmetric load conducting at its full swing. Therefore, replica-feedback biasing dynamically maintains the relation, $V_{DD} - V_{\rm CTRL} = V_{DD} - V_{\rm SWING} = I_{\rm BIAS} \cdot R_{\rm sym}$, against process, temperature, and supply variations. Since the control voltage and the voltage swing are both referenced to the higher supply rail V_{DD}, their potential differences with V_{DD}, $V'_{\rm CTRL} = V_{DD} - V_{\rm CTRL}$ and $V'_{\rm SWING} = V_{DD} - V_{\rm SWING}$, will be used to simplify the forthcoming expressions.

Given the voltage swing $V'_{\rm SWING} = V'_{\rm CTRL}$ and bias current $I_{\rm BIAS}$, the VCO's oscillation period, $T_{\rm vco}$, is expressed as

$$T_{\rm vco} \cong C_b \frac{V'_{\rm CTRL}}{I_{\rm BIAS}} = C_b \cdot R_{\rm sym} \tag{18}$$

where C_b is the total load capacitance seen by the buffer stages in the ring oscillator. The frequency of the self-biased VCO is thus tunable by varying the effective resistance of the symmetric load, $R_{\rm sym}$, with the control voltage $V'_{\rm CTRL}$.

The self-biased PLL claims constant $\omega_n/\omega_{\rm ref}$ ratio by scaling the charge-pump current I_{cp} proportionally with the VCO bias current $I_{\rm BIAS}$ and inversely proportional to the multiplication factor N [11]

$$I_{cp} \propto \frac{I_{\rm BIAS}}{N}. \tag{19}$$

This is realized by replicating the bias current $I_{\rm BIAS}$ via a programmable current mirror, which sets the ratio between I_{cp} and $I_{\rm BIAS}$ according to the desired $\omega_n/\omega_{\rm ref}$ ratio and the multiplication factor N. The PLL in [1] even uses a charge pump which has an almost identical topology to a VCO buffer in order to maximize matching between the two current scalings.

To verify if (19) indeed achieves constant $\omega_n/\omega_{\rm ref}$, we combine (14) and (18) to derive the scaling requirement on I_{cp}

$$\begin{aligned}\frac{1}{I_{cp}} &\propto -\frac{\partial T_{\rm ref}}{\partial V'_{\rm CTRL}} \\ &\cong -N\frac{\partial T_{\rm vco}}{\partial V'_{\rm CTRL}} = -N\frac{\partial}{\partial V'_{\rm CTRL}}\left(C_b\frac{V'_{\rm CTRL}}{I_{\rm BIAS}}\right) \\ &\propto \frac{N}{I_{\rm BIAS}}\left(\frac{\frac{\partial I_{\rm BIAS}}{I_{\rm BIAS}}}{\frac{\partial V'_{\rm CTRL}}{V'_{\rm CTRL}}} - 1\right).\end{aligned} \tag{20}$$

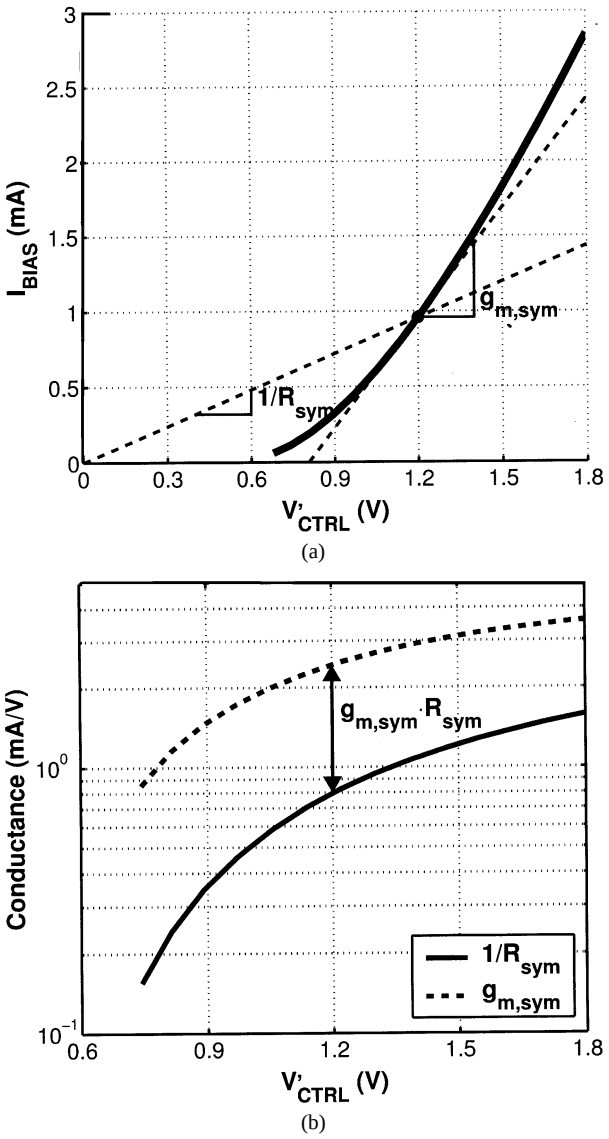

Fig. 8. (a) I–V characteristics of the symmetric load. (b) Scalings of $g_{m,\rm sym}$ and $1/R_{\rm sym}$ and the variation of their ratio, $g_{m,\rm sym} \cdot R_{\rm sym}$.

We find that (19) is in fact an approximation that satisfies adaptive bandwidth only if the relative transconductance of the symmetric load, $(\partial I_{\rm BIAS}/I_{\rm BIAS})/(\partial V'_{\rm CTRL}/V'_{\rm CTRL})$, is constant within the operating range. The relative transconductance is also a ratio between the small-signal transconductance $g_{m,\rm sym} = \partial I_{\rm BIAS}/\partial V_{\rm CTRL}$ and the large-signal conductance $1/R_{\rm sym}$. Also, note that instead of detecting $T_{\rm ref}$, the self-biased PLL adjusts I_{cp} based on $N \cdot T_{\rm vco}$, since it is equal to $T_{\rm ref}$ when the PLL is locked.

Fig. 8 plots the I–V characteristics of the symmetric load and its small-signal and large-signal conductances, $g_{m,\rm sym}$ and $1/R_{\rm sym}$. The small-signal transconductance is the tangential slope on the I–V curve while the large-signal conductance is the slope of the line connecting the origin and the operating point. As seen in Fig. 8(b), the ratio $g_{m,\rm sym} \cdot R_{\rm sym}$, i.e., the gap between the two curves on a log-scale plot, is fairly constant for high $V'_{\rm CTRL}$. However, since the I–V curve is offset from the origin due to the device threshold $V_{\rm TH}$, as the voltage swing $V'_{\rm CTRL}$ approaches $V_{\rm TH}$, $1/R_{\rm sym}$ decreases at a faster rate than

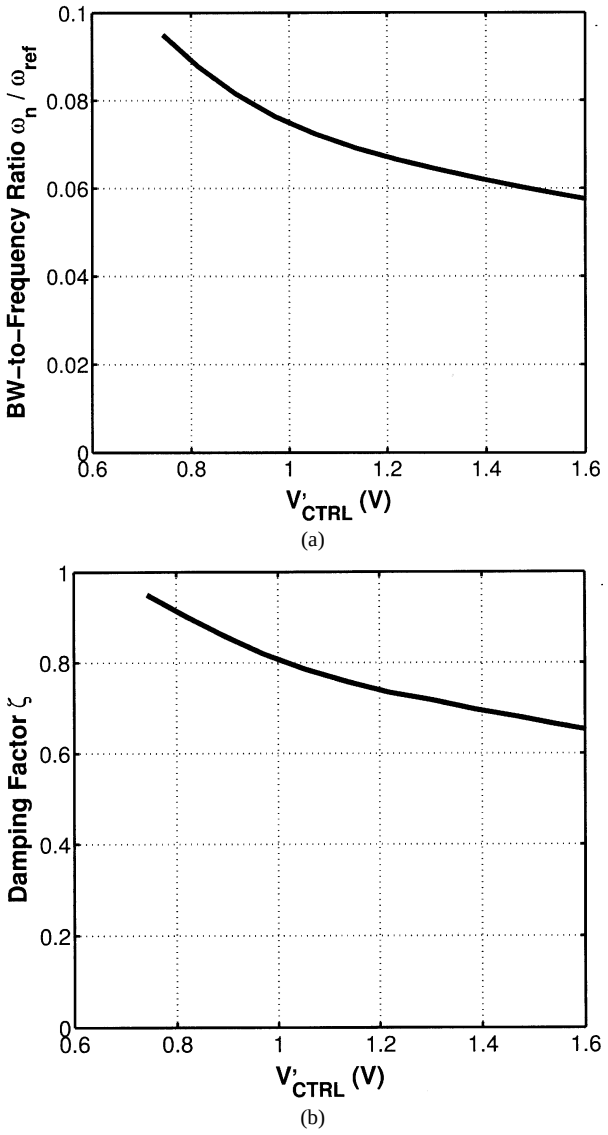

Fig. 9. (a) $\omega_n/\omega_{\rm ref}$ ratio. (b) Damping factor ζ of the self-biased PLL as a function of the voltage swing $V'_{\rm CTRL}$.

$g_{m,\rm sym}$. As a result, the ratio of conductances $g_{m,\rm sym}\cdot R_{\rm sym}$ increases as the voltage swing decreases.

Fig. 9(a) plots the resulting bandwidth-to-frequency ratio $\omega_n/\omega_{\rm ref}$ of the self-biased PLL simulated in a 0.25-μm CMOS technology, which has a nominal supply of 2.5 V and $V_{\rm TH}$ of 0.55 V. In the low-swing regime, the increasing conductance ratio makes the charge-pump current scaling that follows (19) higher than the ideal current in (20). Therefore, the $\omega_n/\omega_{\rm ref}$ ratio, which is fairly constant in the high-swing regime, gradually increases as the voltage swing approaches the device threshold $V_{\rm TH}$. This unwanted variation in $\omega_n/\omega_{\rm ref}$ ratio will be more pronounced in finer-feature CMOS processes, since the nominal supply is scaling down at a faster rate than the threshold voltage is [12]. On the other hand, when the voltage swing is too large, the transistors fall out of the saturation region and the oscillator no longer satisfies (18). Hence, decreasing the supply voltage also limits the high end of the operating range. The frequency range where the $\omega_n/\omega_{\rm ref}$ ratio is kept constant is thus shrinking with CMOS process scaling and this poses a challenge for future adaptive-bandwidth PLL designs.

There are a few possible ways to address this challenge. First, since the difference between $g_{m,\rm sym}$ and $1/R_{\rm sym}$ scalings is basically due to the device threshold $V_{\rm TH}$, one can think of using zero-threshold devices for the symmetric load. Then the $V_{\rm TH}$-offset of the I–V curve in Fig. 8(a) is removed and the variation in $g_{m,\rm sym}\cdot R_{\rm sym}$ is reduced. Second, to cope with the effective reduction in frequency range, one can add a programmable output divider that automatically adjusts its dividing ratio depending on $\omega_{\rm ref}$. For example, when $\omega_{\rm ref}$ is low, the dividing ratio is increased so that the VCO itself can be kept oscillating at a high frequency, while the divider provides the lower-frequency clock. However, this scheme requires *a priori* information on $\omega_{\rm ref}$ or a frequency detector (based on a known fixed reference) that selects an appropriate dividing ratio for each $\omega_{\rm ref}$.

An adaptive-bandwidth PLL must also scale the filter resistance R to keep the damping factor ζ constant. Equation (15) says that R must scale proportionally with $T_{\rm ref}$ or with $N\cdot T_{\rm vco}$. Since $T_{\rm vco}=R_{\rm sym}C_b$ from (18), it follows that R must scale as

$$R\propto N\cdot R_{\rm sym}. \tag{21}$$

The self-biased PLL again approximates $R_{\rm sym}$ with $1/g_{m,\rm sym}$. An additional charge-pump injects a current $I_{cp,2}$ onto the node V_{FF} in Fig. 7, while the PD error pulse is asserted. This current then develops a voltage offset between $V_{\rm CTRL}$ and $V_{\rm SWING}$, which is proportional to $I_{cp,2}/g_{m,\rm sym}$. Therefore, the self-biased PLL effectively scales the filter resistance R as the small-signal resistance of the replica symmetric load, $1/g_{m,\rm sym}$. The dependency of R on the multiplication factor N can be implemented either by a programmable current mirror that adjusts the ratio between the second charge-pump current $I_{cp,2}$ and $I_{\rm BIAS}$ or by a sampled feedforward filter which holds the sampled error charge for the entire reference cycle $N\cdot T_{\rm vco}$ [11]. The latter is more desirable to reduce the reference spur on the output clock, especially if N is large.

Similar to the case of the charge-pump current, the approximation $R_{\rm sym}\propto 1/g_{m,\rm sym}$ made by the self-biased PLL is valid only in the high-swing regime. Fig. 9(b) plots the variation of the damping factor of a self-biased PLL with respect to $V'_{\rm CTRL}$. While the damping factor ζ is fairly constant for large voltage swings, it gradually increases as the $V'_{\rm CTRL}$ approaches $V_{\rm TH}$. Since the nonideal scalings of I_{cp} and R are both due to the variation in the relative transconductance of the symmetric load, $g_{m,\rm sym}\cdot R_{\rm sym}$, the aforementioned solutions can also help extend the frequency range in which the damping factor is constant.

B. Regulated-Supply PLLs With CMOS Inverters

Fig. 10 illustrates the VCO and its supporting bias generator of a regulated-supply PLL, proposed in [2]. The VCO is made up of CMOS inverters and the bias generator is basically a linear voltage regulator that controls the VCO supply to adjust its frequency and to reject unwanted noise from the external supply. Similar to the self-biased PLL, the control voltage $V_{\rm CTRL}$ sets the desired voltage swing of the oscillator and a bias generator adjusts the supplied current $I_{\rm BIAS}$ so that the voltage swing $V_{\rm SWING}$ matches $V_{\rm CTRL}$. Unlike a differential stage, a

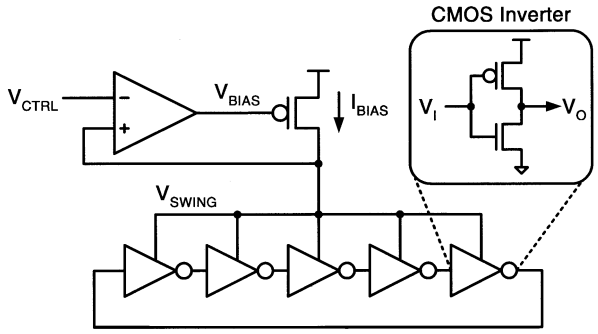

Fig. 10. The inverter-based VCO and its supporting biasing generator of the regulated-supply PLL.

CMOS inverter does not dissipate constant current and there exists no replica that can model the effective resistance of the VCO, $R_{\rm inv} = V_{\rm SWING}/I_{\rm BIAS}$. Therefore, the feedback-biasing circuitry directly regulates the voltage swing of the oscillator, $V_{\rm SWING}$. Stabilizing its feedback can be an issue since both the nodes $V_{\rm SWING}$ and $V_{\rm BIAS}$ have high capacitance. For example, the PLL in [2] sufficiently reduced the resistance seen on $V_{\rm SWING}$ to make the pole associated with $V_{\rm BIAS}$ node dominant, and the PLL in [3] used a compensating capacitor to achieve the same. An inverter-based VCO has large voltage swings and sharp transitions, which are advantageous for reducing jitter [9], but an inverter is inherently a single-ended buffer that cannot reject common-mode noise.

The regulated-supply PLL achieves adaptive bandwidth by applying similar design principles to those of the self-biased PLL. Equations (18)–(21) still hold for the regulated-supply PLL except that $V'_{\rm CTRL}$ and $V'_{\rm SWING}$ in the expressions are replaced with $V_{\rm CTRL}$ and $V_{\rm SWING}$, respectively, as both the control voltage and the voltage swing are referenced to ground. The charge-pump current I_{cp} is scaled proportional to $I_{\rm BIAS}/N$ and the filter resistance R is scaled proportional to $N/g_{m,\rm inv}$ using a second charge-pump injecting current onto the node $V_{\rm SWING}$, where $g_{m,\rm inv}$ is the small-signal conductance of the VCO seen at the node $V_{\rm SWING}$. As in the self-biased PLL, the regulated-supply PLL then achieves constant $\omega_n/\omega_{\rm ref}$ and ζ by relying on the fact that the relative transconductance $g_{m,\rm inv} \cdot R_{\rm inv}$ is constant, i.e., that $g_{m,\rm inv}$ is proportional to $1/R_{\rm inv}$.

Therefore, the regulated-supply PLL suffers from similar limitations to those of the self-biased PLL. Fig. 11 plots the normalized bandwidth $\omega_n/\omega_{\rm ref}$ and the damping factor ζ of the regulated-supply PLL simulated in a 0.25-μm CMOS process. The $\omega_n/\omega_{\rm ref}$ ratio and ζ are fairly constant for high $V_{\rm CTRL}$, but the slope steepens as $V_{\rm CTRL}$ approaches $V_{\rm TH}$, for the same reasons as seen in the self-biased PLL. To mitigate this problem, the designers of the regulated-supply PLLs have varied the channel lengths of the charge pump's current source devices to find the I–V characteristics that can minimize the variation in $\omega_n/\omega_{\rm ref}$. However, this *ad hoc* solution is sensitive to process variations, environmental conditions, and the correctness of the device models. Also, the highest voltage swing is limited by the saturation requirement of the current source in the bias generator. Hence, as CMOS processes scale down and the V_{DD}-to-$V_{\rm TH}$ ratio decreases, the effective frequency range of the regulated-supply PLL will be narrowed.

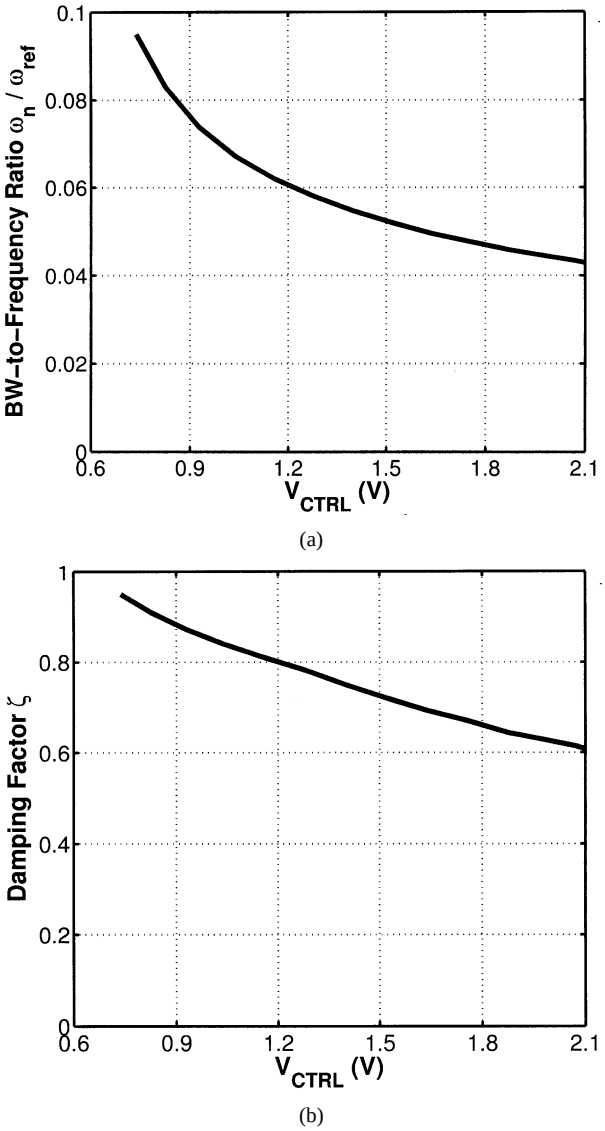

Fig. 11. (a) The $\omega_n/\omega_{\rm ref}$ ratio and (b) the damping factor ζ of the regulated-supply PLL as a function of the voltage swing $V_{\rm CTRL}$.

V. Estimation of the PLL/DLL Open-Loop Parameters

This section describes how to estimate open-loop gains, i.e., C_ω and C_ϕ for PLLs and C_D for DLLs, from a time-domain transient response, so that one can verify the bandwidth scaling after the PLL/DLL is designed or fabricated. There are a few other methods to characterize a PLL/DLL, but the time-domain characterization is the most general and can be used for both simulation and measurement results. For example, one can estimate open-loop gains of a PLL by evaluating (12) and (13) after measuring the individual parameters such as VCO gain, charge-pump current, filter resistance, etc. Although straightforward in simulation where each PLL block is accessible, it is impossible to measure them after the PLL has been fabricated. Another method is to measure the frequency response of the PLL, by sweeping the frequency of a sinusoidal phase noise source purposely added to the input and observing the resulting output phase. This approach is most commonly used in testing equipments, but it is time-consuming to do the same using SPICE [10]. Previous time-domain characterizations are mostly based

on closed-loop responses [6], where a certain linear model is assumed and its model parameters are estimated by least-squares fitting [16]. Unfortunately, this estimation is often inaccurate, especially when the loop is overdamped. It is because the purpose of a feedback is to desensitize the system's response from its parameter variations and, thus, the closed-loop response of a well-designed PLL is not a sensitive measure of its parameters. To overcome these limitations, this section introduces a method of using the discrete-time, open-loop impulse function to characterize a PLL/DLL. First, ways to measure the open-loop impulse function of a PLL/DLL, directly or indirectly, are described. Then, we discuss how to estimate the open-loop gains from the impulse response.

One of the easiest ways to construct the impulse response from the input/output transients is to use deconvolution. Once the time-sequences of the input phase $\phi_{\rm ref}[n]$ and the output phase $\phi_{\rm out}[n]$ are measured, the phase error $\phi_{\rm err}[n] = \phi_{\rm ref}[n] - \phi_{\rm out}[n]$ is calculated and the impulse transfer function $h[n]$ is derived by

$$h[0] = \frac{\phi_{\rm out}[0]}{\phi_{\rm err}[0]}$$
$$h[n] = \frac{\phi_{\rm out}[n] - \sum_{k=0}^{n-1} h[k]\phi_{\rm err}[n-k]}{\phi_{\rm err}[0]}, \quad n \geq 1 \qquad (22)$$

where it is assumed that the system is causal and the input and output settle to 0 before $n = 0$ [15]. The impulse response of a DLL can be derived similarly by using $D_{\rm err}[n]$ and $D_{\rm out}[n]$ as the input and output variables of the open-loop system, respectively. Since noise on the early samples of the input and output sequences can largely distort $h[n]$, one can use an averaged response over multiple measurements when estimating $h[n]$ from noisy data.

Alternatively, the impulse response of a PLL/DLL can be directly measured in simulation or experimentally measured by physically disabling the feedback momentarily. For example, the phase detector outputs can be gated so that the PLL/DLL runs in open-loop for a fixed time interval. The response of the PLL/DLL during that period is then the impulse response scaled by the error applied at the beginning of the period. Caution should be taken when measuring the open-loop response of a PLL since its impulse response is unbounded. It must be ensured that the PLL is locked before disabling the feedback and that the disabling period is short enough so that the VCO frequency does not reach its tuning limits. On the other hand, no such caution is required for a first-order DLL since it has a bounded open-loop impulse response. If no initial error is applied, the setup for measuring the open-loop response can also measure the noise characteristics of the PLL, e.g., the phase noise of the VCO and its clock buffers. By measuring the rms jitter correlations at different time points, it may even be possible to estimate each noise contribution separately, e.g., the flicker noise and thermal noise of the VCO [9].

Note that the aforementioned methods to estimate the open-loop impulse response $h[n]$ do not assume a particular system order for the PLL/DLL under test. They assume only that the PLL/DLL is a causal, linear time-invariant system. Thus, they can be generally applied to linear PLL/DLLs with orders higher than two and can even help identify their high-order effects. The rest of this section describes how to estimate the open-loop gains from the impulse response $h[n]$ and how to identify some of the high-order effects.

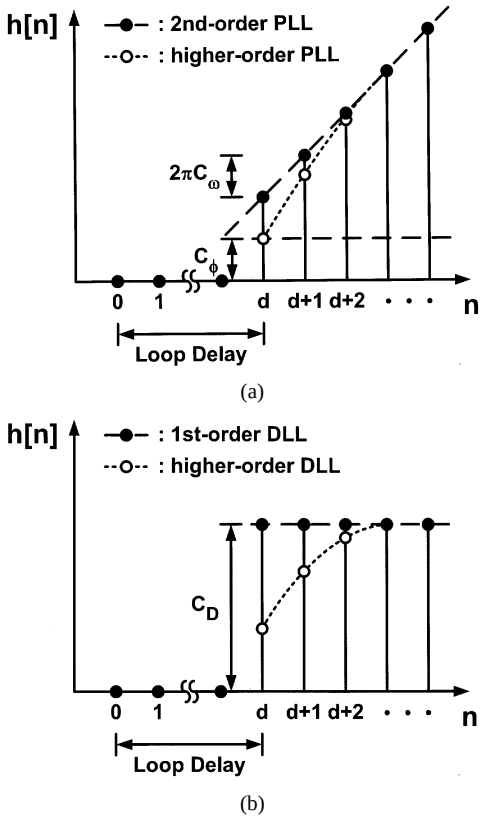

Fig. 12. Discrete-time, open-loop impulse responses of a PLL. (a) DLL. (b) Estimation of their loop parameters.

Fig. 12 shows the open-loop impulse responses of a PLL and a DLL obtained from simulation. In case of the PLL, the impulse error gives rise both to the phase ϕ_P and frequency ω_I. The rise in ϕ_P appears as the initial rise in $\phi_{\rm out}$ which stays constant for the rest of the period. On the other hand, the rise in ω_I appears as a constant increase in $\phi_{\rm out}$. Therefore, from the impulse response shown in Fig. 12(a), we can estimate the open-loop gain C_ω from the asymptotic slope of $h[n]$ and C_ϕ from the first nonzero sample subtracted by $2\pi C_\omega$. The impulse response also reveals information on more complex behavior of the PLL. For example, the position of the first nonzero $h[n]$ sample indicates the loop delay of the PLL. Also, if $h[n]$ does not increase linearly after its first nonzero sample, it means that the system contains higher order poles. With this additional information on loop delay and higher order poles, more sophisticated stability analysis than just using ω_n and ζ is possible.

The impulse response of a DLL is simpler than that of the PLL, as shown in Fig. 12(b). In response to an impulse error, the output delay $D_{\rm out}$ changes in a step. The gain C_D is then estimated from the size of this step. As in the PLL case, the loop delay and the high-order poles can be estimated from the position of the first nonzero $h[n]$ sample and the nonideal transient of $h[n]$, respectively. The simplicity of the DLL behavior

makes it even possible to estimate C_D and ω_n upon inspection of the time-domain transient.

VI. Conclusion

This paper described a general design methodology for adaptive-bandwidth PLLs and DLLs. We first derived the discrete-time, open-loop dynamic model of the PLL and DLL that characterizes the change in the output variables in response to the sampled error. The phase and frequency of the PLL is updated each cycle by the sampled phase error scaled by C_ϕ and C_ω, respectively. Similarly, the delay of the DLL is updated each cycle by the sampled error scaled by C_D. The adaptive-bandwidth criteria are then expressed in terms of these open-loop gains, simply as constant C_ϕ and C_ω for PLLs and a constant C_D for DLLs. By applying these criteria to the previously published charge-pump PLL/DLLs, we found that the self-biased PLL/DLL and the regulated-supply PLL/DLL rely on the small-signal transconductance $g_{m,\mathrm{vco}}$ tracking the large-signal transconductance $1/R_{\mathrm{vco}}$ to satisfy the scaling equations of the charge-pump current and filter resistance in (14) and (15). This approximation, however, holds only when the voltage swing of the VCO/VCDL is sufficiently higher than the device threshold V_{TH} and presents design challenges in sub100-nm CMOS processes.

Therefore, there remains a need to design a better adaptive-bandwidth PLL/DLL that can extend to next generations of CMOS processes. This paper suggested the use of zero-V_{TH} device to mitigate the tracking problems of $1/g_{m,\mathrm{vco}}$ and R_{vco}, and the use of dynamically adjusting output dividers to constrain the VCO's operating range. Direct implementation of (14) may be possible if realized digitally with some form of background calibration. In fact, digital or semidigital implementations are expected to prevail in the near future as the gate leakage of MOS capacitors and the subthreshold leakage of MOS switches pose potential problems to the use of charge pumps. The open-loop dynamic equations in (8) and (11) are general enough to guide the design of such digital PLL/DLLs.

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