A Comprehensive Phase-Transfer Model for Delay-Locked Loops

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***Abstract* - This paper presents a comprehensive model for analyzing the behavior of an analog delay-locked loop (DLL). Unlike previous models, the proposed version includes both constant and variable phase-offset terms, making it possible to calculate jitter transfer characteristics, stability, and static phase errors from a single unified model. The topology more closely approximates the underlying architecture of the DLL, resulting in improved accuracy and enabling better tradeoffs between bandwidth, stability, and power.**

Introduction

Delay-locked loops (DLLs) have become increasingly common in signal alignment applications, where they offer lower power consumption and better supply-noise immunity and stability than an equivalent phase-locked loop. However, several important tradeoffs must be made in the design of a DLL, including bandwidth vs. stability and power vs. jitter. To understand these tradeoffs and create an optimal design, accurate modeling of the DLL is essential.

Many of the early continuous-time delay-locked-loop models were derived from a linearized PLL model based on the assumption that a three-terminal voltage-controlled delay line (VCDL) could be modeled as a two-terminal device [1]. However, transfer functions derived from this model are missing the feed-forward zero contributed by the input-signal connection, and therefore have a single-pole roll-off instead of a slightly peaked response.

More recently, a z-domain model was published that accounts for the third connection, but overestimates peaking in the frequency response [2]. In this model, the VCDL delay block is placed inside the feedback loop of the DLL, which delays the control signal by an extra clock period. As a result, jitter-peaking increases, and the system appears less stable.

In this paper, a Laplace-domain DLL model is introduced that more accurately predicts jitter peaking and system stability, and can be used to derive the transfer characteristics of jitter generated in the input buffers and VCDL. A simplified z-domain version of the model is also presented, which can be used to model sampled systems and to analyze stability using root-locus techniques.

Model Topology

A simplified block diagram of the proposed Laplace-domain DLL model is shown together with the models from [1] and [2] in Fig. 1. In these models, ϕ_{ref}, ϕ_{buf} and ϕ_{dl} are all sources of jitter that originate in the clock source, input buffers, and VCDL, respectively. ϕ_e is the phase error, τ_{dl} is the nominal delay through the VCDL, τ_{buf} is the combined propagation delay of the input buffers, H_f is the filter transfer function, and n is the nominal number of clock cycles separating the output and reference signals.

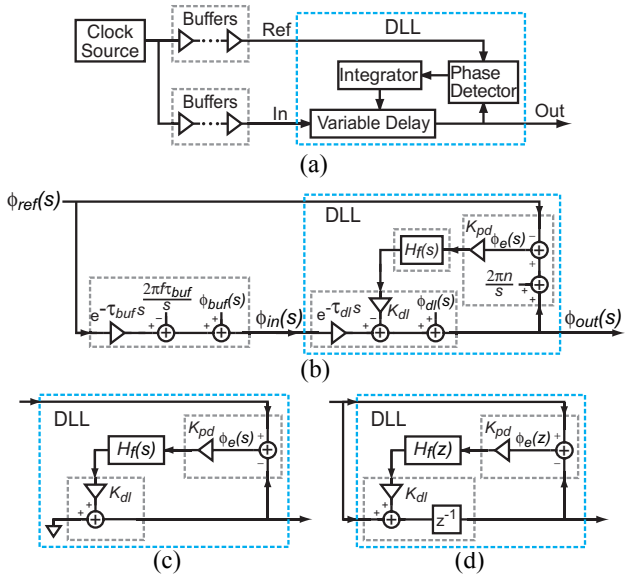

Fig. 1: (a) Basic delay-locked loop architecture with system interconnections and different linearized models of system: (b) proposed model (c) model from [1] (d) model from [2].

An important distinction between this model and previously published models is the representation of delays with separate magnitude and phase terms. In a phase-transfer model, the waveforms being delayed are phases, not voltages, so any delay in the system will both increase the magnitude of the phase signal and delay the phase waveform. Furthermore, the magnitude and phase terms refer to different frequencies: the frequency of the clock source (which is generally assumed to be constant) and the frequency of the phase waveform (which depends on $s = j\omega$). Changes in the magnitude of the phase are with reference to the fixed clock frequency, whereas changes in the delay of the phase waveform are with reference to the modulation frequency. To accurately capture both of these effects, delays must be modeled with both a constant-phase offset term to account for changes in phase magnitude and a complex exponential gain term to account for the delay of the phase waveform.

Another important difference is the placement of the

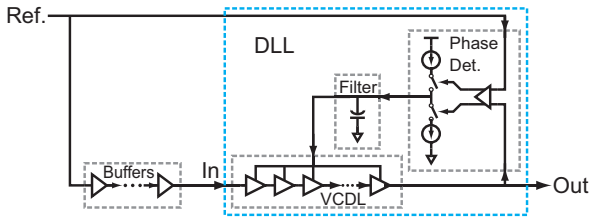

Fig. 2: First order charge-pump DLL.

VCDL exponential-delay block outside of the feedback loop. This was done to account for the fact that in most DLLs, changes in the control voltage immediately alter the delay through the VCDL. Even signals that have propagated part way through the delay line when the control voltage changes will be affected by the remaining buffers. The placement outside of the feedback loop significantly alters the stability of the system, and can affect many important design tradeoffs.

The phase detector in the proposed model has also been modified to compensate for the n-cycle offset between the reference and output signals. Most DLLs operate with a nominal VCDL delay of one clock period, which means the phase detector is comparing edges from adjacent clock periods. To compensate for the offset, a correction factor of $2\pi n/s$ is subtracted from one of the phase-detector inputs, causing the DLL to increase the VCDL delay by n clock periods. The fixed offset makes it possible to accurately calculate the magnitude of any static phase errors without altering the stability of the DLL.

Jitter Transfer Characteristics

A. Phase Transfer Function

To understand the differences between the proposed model and the model in [2], the first-order charge-pump DLL shown in Fig. 2(a) is analyzed. A relatively simple example was chosen to clearly demonstrate the differences, although the model can easily be extended to higher order DLLs and digital DLLs. From Fig. 2(b), the reference-output jitter transfer function is

$$\frac{\phi_{out}(s)}{\phi_{ref}(s)} = \frac{e^{-(\tau_{buf}+\tau_{dl})s} + K_{pd}K_{dl}H_f(s)}{1 + K_{pd}K_{dl}H_f(s)} \quad (1)$$

$$= \frac{1 + (s/w_p)\cdot e^{-(\tau_{buf}+\tau_{dl})s}}{1 + (s/w_p)}, \quad (2)$$

which has a pole at

$$w_p = \frac{I_{cp}K_{dl}}{2\pi C}, \quad (3)$$

where C is the shunt capacitor integrator, and I_{cp} is the charge-pump current. The corresponding buffer-output (ϕ_{out}/ϕ_{buf}) and delay-line-output (ϕ_{out}/ϕ_{dl}) transfer functions are

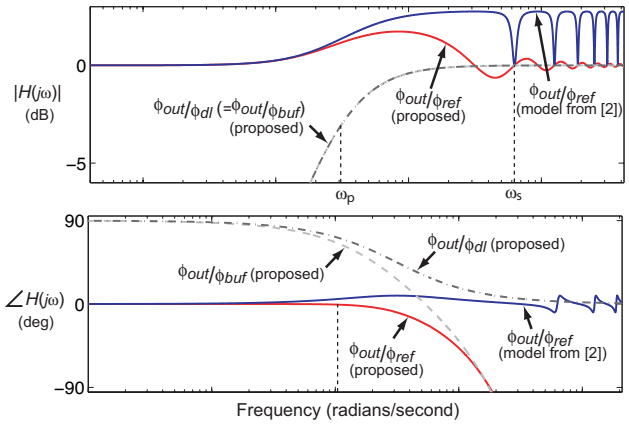

Fig. 3: Frequency response of a first order charge-pump DLL using the proposed model and the z-domain model from [2].

$$\frac{\phi_{out}(s)}{\phi_{buf}(s)} = \frac{e^{-\tau_{dl}s}}{1 + K_{pd}K_{dl}H_f(s)} = \frac{(s/w_p)\cdot e^{-\tau_{dl}s}}{1 + (s/w_p)} \quad (4)$$

and

$$\frac{\phi_{out}(s)}{\phi_{dl}(s)} = \frac{1}{1 + K_{pd}K_{dl}H_f(s)} = \frac{(s/w_p)}{1 + (s/w_p)}. \quad (5)$$

All three transfer functions are plotted in Fig. 3, along with the ϕ_{out}/ϕ_{ref} response of the z-transform model from [2]. In this example ω_p is set to 5% of the loop sample rate (ω_s). The jitter peaking predicted by [2] is similar to that of the proposed model at lower frequencies, but then begins to diverge above ω_p. The difference is caused by the sampling behavior of the z-transform, which allows high frequency jitter to alias into the passband of the DLL. The phase response in [2] also diverges at higher frequencies, and is missing the expected roll-off above ω_p. The missing roll-off is a result of the misplacement of the exponential delay term *after* ϕ_{out}, which creates a direct (undelayed) path from input to output.

Another important observation from Fig. 3 is that jitter induced by power supply noise in the buffers and VCDL exhibits no peaking, and is attenuated below ω_p. Thus, this source of jitter can be minimized by setting the tracking bandwidth as high as possible. However, increasing the tracking bandwidth may also make the DLL more susceptible to jitter on the reference clock. Consequently, a tradeoff must be made between susceptibility to reference clock jitter and susceptibility to power-supply noise coupling.

B. Comparison With Functional Model

To verify the accuracy of the proposed model, a functional model of a first-order analog DLL with a multiplying phase detector is analyzed. The model, shown in Fig. 4, is implemented in Simulink using basic library elements and components from the communications and digital-signal processing blocksets. The analog phase detector consists of an ideal $\pi/2$ phase shifter, a multiplier block, scaling elements,

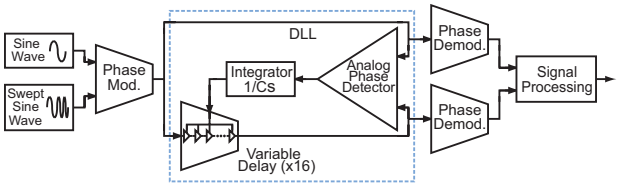

Fig. 4: Simplified functional model of first order analog DLL.

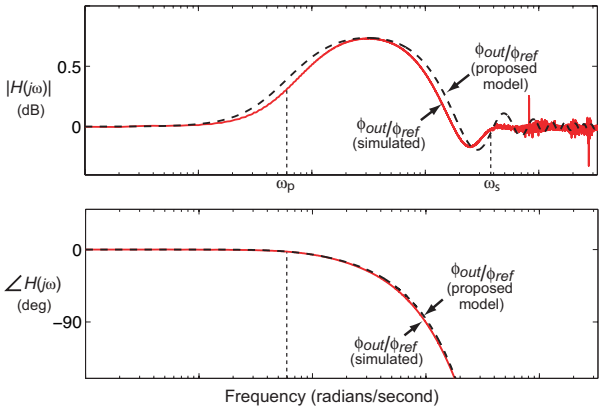

Fig. 5: Calculated and simulated frequency response of first order DLL with analog (multiplying) phase detector ($\omega_p = \omega_s/62.8$).

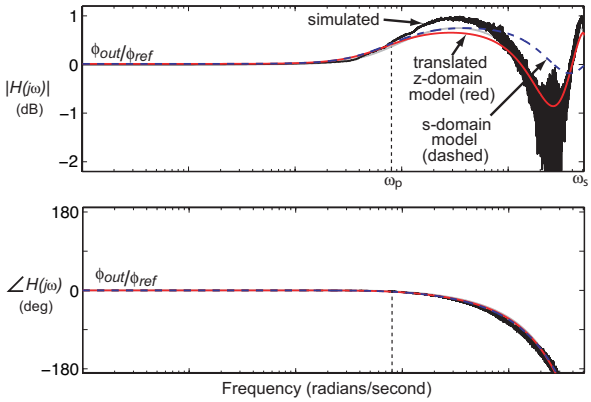

Fig. 6: Frequency response of a first order charge-pump DLL.

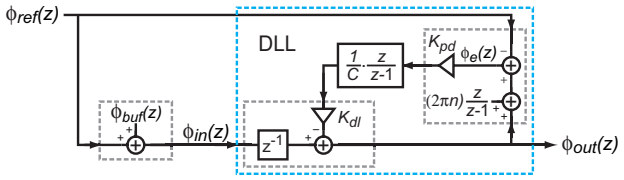

Fig. 7: Simplified z-domain model of first order charge-pump DLL.

and a third-order Butterworth lowpass filter to remove the image spectrum [3].

Using the functional model, an approximate ϕ_{out}/ϕ_{ref} phase-transfer response can be calculated by driving the reference input with a swept sinusoidal jitter signal and dividing the output and input spectrums. In the resulting response curves, plotted in Fig. 5, the simulated response matches that of the proposed Laplace-domain model over a wide range of frequencies. In contrast, the z-transform model in [2] overestimates jitter peaking at higher frequencies.

For charge-pump type DLLs a similar analysis can be performed. The functional model of a first-order charge-pump DLL has the same basic architecture described above, but with a pulse-width modulator (PWM) to perform phase detection. The PWM phase detector employs flip-flops and a NAND gate to create variable-width digital pulses whose area is proportional to the phase difference between the inputs [3]. Unlike the multiplier described earlier, most PWM phase detectors are edge-triggered, and therefore perform a sampling operation. As a result, jitter from higher frequencies can mix down into the passband, creating ripple in the magnitude response.

A plot of the simulated phase-transfer response of the charge-pump DLL is shown in Fig. 6. The magnitude response matches well through the first jitter peak, although the amplitude is slightly low. The difference is caused by small delays introduced by the blocks used to implement the functional model. At higher frequencies, the sampling creates ripples in the magnitude response that are not reproduced by the Laplace-domain model. The mismatch is a result of the continuous-time nature of the Laplace-domain model, which only approximates the sampling operation.

For the charge-pump DLL, a better match is achieved with a discrete-time z-domain version of the proposed model. Using impulse invariance, each element in the Laplace-domain model can be translated directly to the z-domain to form an equivalent model. In the resulting model, shown in Fig. 7, the z^{-1} exponential delay block is again placed outside of the feedback loop.

Using the translated model, the phase-transfer response of a first order charge pump DLL is calculated, and the results plotted together with the simulated transfer function in Fig. 6. As can be seen in the plot, the ripples in the magnitude response are now accurately rendered throughout the entire frequency range.

Stability Analysis

An important difference between the proposed model and the model in [2] is the stability of the feedback loop. Fig. 8(a) shows a simplified z-domain model of the feedback loop in a first-order charge-pump DLL. The exponential delay term is correctly placed outside of the feedback loop where it has no effect on stability. In contrast, the equivalent model from [2] has an exponential delay term inside the feedback loop. The additional delay term, shown in Fig. 8(b), alters the open-loop transfer function of the DLL and makes the system appear less stable.

A plot of the corresponding root-loci for both models is shown in Fig. 9. As can be seen in the plot, proper placement of the delay terms significantly improves the stability predicted by the model. Consequently, some DLLs that previously

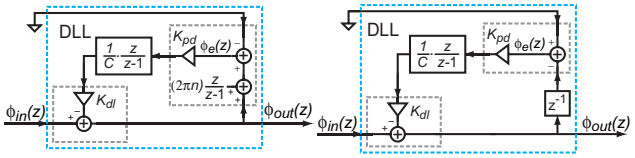

Fig. 8: Simplified z-domain model of the feedback loop in a first order charge-pump DLL: (a) proposed (b) model from [2].

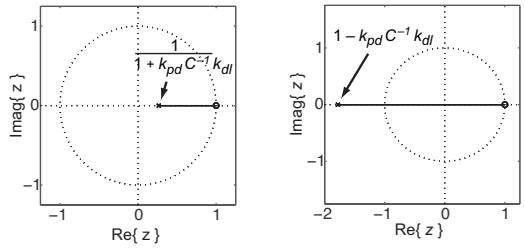

Fig. 9: Root-locus plot of first order charge-pump DLL using (a) proposed model and (b) the model from [2].

appeared to be conditionally stable are actually unconditionally stable. This has important implications in the design of DLLs, where tracking bandwidth is sometimes constrained by stability requirements.

Design Example

To highlight the importance of model accuracy on design tradeoffs, the second-order charge-pump DLL described in [2] is re-analyzed using the proposed model. The previous analysis established limits on the cutoff frequency of the loop filter to attenuate jitter while maintaining stability. However, because the model overestimates jitter, the actual benefit of the filter is much less than predicted. Furthermore, the minimum filter cutoff frequency is limited by stability margins, which are degraded by the misplaced delay block in the feedback loop.

The difference between the two models is clearly visible in the open-loop frequency response curves shown in Fig. 10. The phase margin calculated with the proposed model is larger than the margin in [2], and as the loop gain is increased, the difference becomes even greater. If the loop filter is omitted, the phase margin of the proposed model approaches 90 degrees, and is limited only by higher order poles and any propagation delays in the feedback loop.

The difference between the proposed model and the model in [2] becomes more pronounced as the tracking bandwidth is increased. The effect can be seen in Fig. 11, which shows the phase margin as a function of tracking bandwidth, with and without a loop filter. In the plot, the phase margin of the proposed model exceeds 30 degrees until the tracking bandwidth reaches 9% of the loop sample rate. In contrast, to achieve the same phase margin with [2], the tracking bandwidth would be limited to approximately half that value. When the loop filter is removed, the bandwidth can be increased even further before stability limits are reached.

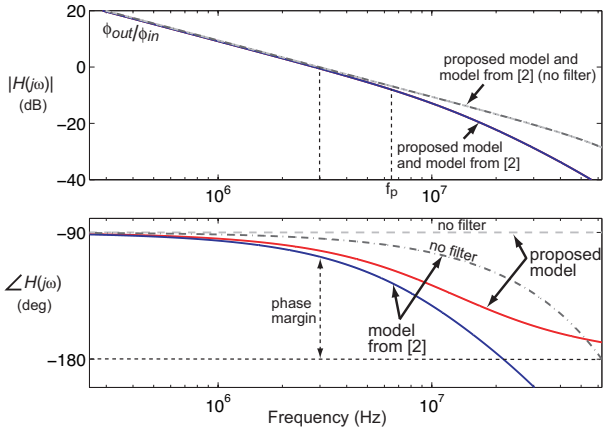

Fig. 10: Open-loop frequency response of first and second order charge-pump DLL from [2], with and without loop filter.

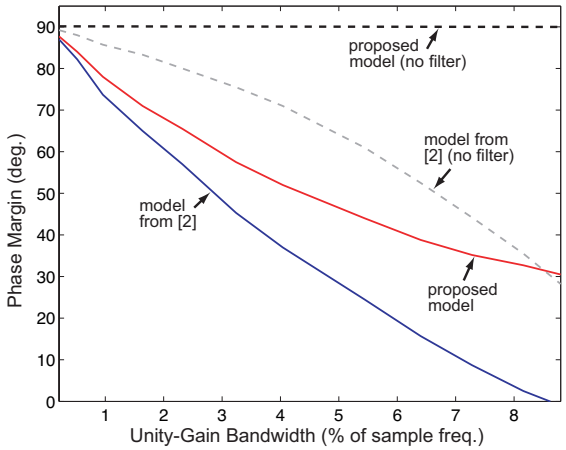

Fig. 11: Phase margin as a function of unity-gain bandwidth.

Conclusion

The analytical model presented in this paper provides a comprehensive tool for analyzing the frequency response, static phase errors, and stability of delay-locked loops. The structure of the model is carefully matched to the underlying architecture of the DLL, giving it better accuracy than previously published models. The improved accuracy makes it possible to increase the tracking bandwidth and achieve better performance while still maintaining adequate stability margins.

References

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