An Area-Efficient 8-Bit Single-Ended ADC With Extended Input Voltage Range

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***Abstract*—This brief presents an 8-bit successive approximation register analog-to-digital converter (ADC) implemented within a system-on-chip (SoC) for autonomous flapping-wing microrobots. The ADC implements hybrid split-capacitor sub-digital-to-analog converter (DAC) techniques to achieve 35.72% improvement in a capacitor bank energy-area product. The device also implements an extended single-ended input voltage range allowing a direct connection to sensors while maintaining low-power operation. This technique allows 51.7% DAC switching energy reduction compared to the state of the art. The SoC, fabricated in 40-nm CMOS, includes four parallel 0.001 mm^2 1 MS/s ADC cores multiplexed across 13 input ports. It enables 0 to 1.8-V input range while operating off of a 0.9 V supply. At 1 MS/s, the ADC achieves a signal-to-noise and distortion ratio of 45.6 dB for a 1.6-V_{pp} input signal and consumes 10.4 μW.**

***Index Terms*—Analog-to-digital converter (ADC), successive approximation register (SAR), extended input voltage range.**

I. Introduction

FLYNG microrobots such as Harvard's RoboBee [1] are severely power and weight constrained applications that rely on capturing and processing wide voltage range single-ended analog inputs from various sensors (e.g., optical flow camera, accelerometer, gyroscope, etc.) to enable autonomous flight. To facilitate integration within a multicore "brain" system-on-chip (SoC) for controlled flight [2], this brief presents an 8-bit successive approximation register (SAR) analog-to-digital converter (ADC) that offers low energy-area product (EAP) to minimize ADC footprint and extended single-ended input range 2× the power supply voltage to enable direct connection to sensors.

Many techniques have been presented to reduce SAR ADC power, but most reduce power consumption at the expense of increased area. Van Elzakker *et al.* [3] proposed stepwise charging, which requires an energy saving capacitor bigger than the rest of the ADC including the DAC capacitor array. Tai *et al.* [4] proposed a subranging SAR ADC that requires a larger unit capacitor than a standard SAR albeit with relaxed matching requirements. To reduce EAP, Yip and Chandrakasan [5] proposed to combine a power-saving, split-capacitor switching algorithm [6] and a sub-DAC topology to save area. However, strictly combining these two techniques does not yield the best area or the best power, as this brief will demonstrate.

Liu *et al.* [8] proposed the complex one-side switch method (COSS). The proposed method requires a differential input and the availability of a precise Vref/2 supply for the ADC. To fully realize the benefit of COSS, the Vref/2 voltage needs to be generated by a lossless mechanism.

Other designs have sought to improve dynamic range of operation. Hu *et al.* [7] showed an 8-bit single-ended SAR ADC with an input range higher than V_{DD}, but the ADC architecture limits the input range to 1.3 V on a 1.1 V supply, thus limiting input voltage range improvement. Tsai *et al.* [9] increased input common mode range via a dual voltage domain SAR ADC, but the input signal amplitude remains limited by the low voltage domain. Han *et al.* [10] proposed dynamic range folding to achieve an input range of $2V_{DD}$. However it requires a large sampling capacitor to mitigate the effect of charge injection and dynamic range folding.

To enable direct sensor connection to the SoC powered off a 0.9V supply (V_{DD}), 1.8V analog input range is desirable. This brief introduces a hybrid, extended-range DAC design comprising (i) a hybrid combination of split-capacitor and sub-DAC techniques to further reduce area and power consumption compared to [5] and (ii) an extended-range technique that doubles the single-ended input voltage range while operating off of a low V_{DD} to maintain power savings. Section II describes the proposed hybrid split-capacitor sub-DAC technique and the proposed extended input range technique. Simulation results confirm their benefits. Section III presents the implementation of the ADC subsystem inside the RoboBee "Brain" SoC in 40nm CMOS and important implementation details of the ADC. Silicon results are given in Section IV. Finally, Section V concludes this brief.

II. ADC Techniques

A. Hybrid Split-Capacitor Sub-DAC

The hybrid split-capacitor sub-DAC technique removes the area penalty of a strict split sub-DAC implementation—the second sub-DAC—while improving the switching energy required. Figure 1 compares an 8b DAC implementing the proposed hybrid technique to a strict implementation [5], which requires two identical sub-DACs. First, the hybrid DAC removes the MSB sub-DAC and replaces the coupling

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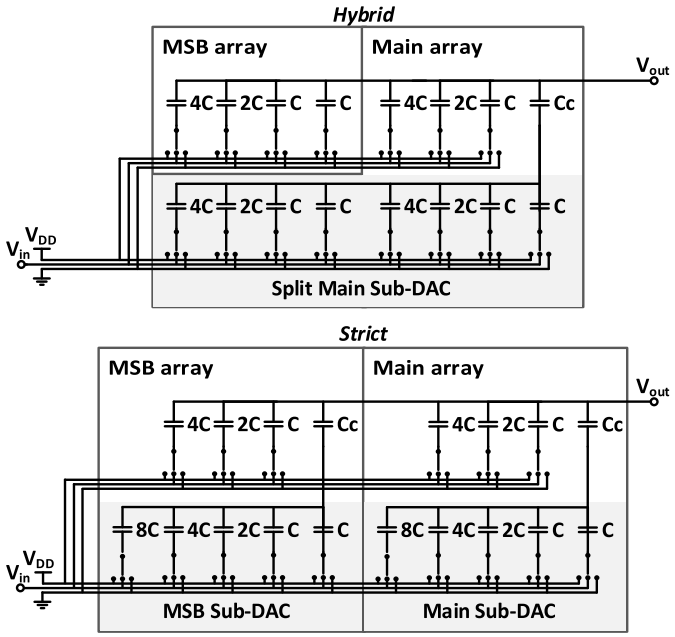

Fig. 1. Hybrid implementation of the split-capacitor and sub-DAC techniques showing 1/3 reduction in capacitor area compared to a strict implementation.

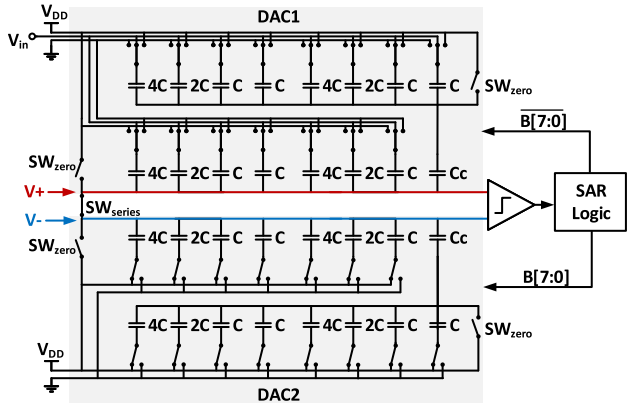

Fig. 2. Extended range SAR ADC built from two series connected hybrid DACs, a comparator, and SAR logic. Sample phase shown.

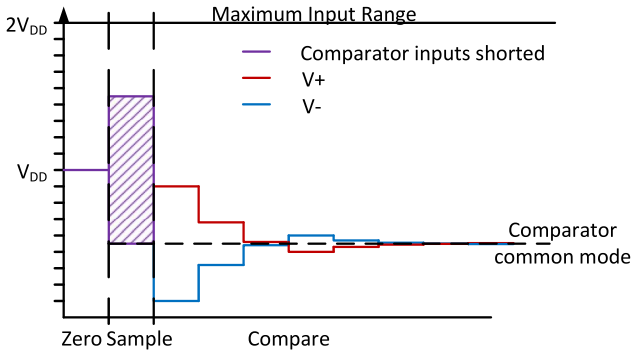

Fig. 3. Comparator input voltage during DAC zeroing, sampling, and comparison phase. Dashed area represents the possible comparator input voltage during sampling. Purple indicates the two inputs are tied together.

capacitor (C_C) in the MSB array with a unit capacitor (C). Second, it splits out the 8C from the *main sub-DAC* to create the *split main sub-DAC* shown. Assuming the value of C_C is on the order of C, the area of a strict implementation is $A_{strict} = (2^M + 2^{S+1})C$ where M is the number of bit of the main DAC and S the number of bit of the sub-DAC. For the hybrid technique, the equation is $A_{hybrid} = (2^M + 2^S)C$. As a result, the area for a single-ended 8b DAC with 4b sub-DACs decreases from 48C to 32C, removing 33.3% of the original capacitor area. Overall, the hybrid implementation significantly reduces total ADC area since the capacitor banks consume a large fraction of area in a SAR ADC.

The hybrid DAC does not compromise mean switching energy and is 3.5% lower than in the strict implementation. The switching algorithm follows the split capacitor algorithm from [6] however a "conventional" transition [6] occurs when the LSB capacitor of the MSB array must be lowered. Despite this "conventional" transition, the overall switching energy is lower. During the operation of the Split Main Sub-DAC less charge need to move compared to [5] which performs the split capacitor method on two sub-DACs connected through two coupling capacitors. Hence, the hybrid DAC procures a slight energy reduction.

B. Extended Input Range

In order to extend the single-ended input range, two hybrid DACs (Fig. 2) are combined in a pseudo-differential bipolar manner; with the two DACs connected in series through a switch (SW_{series}) and DAC2 referenced to V_{DD} during sampling similar to the dynamic folding range technique [10]. In this configuration, DAC2 does not need a V_{in} input since it is not used for single-ended operation.

Figure 3 shows the evolution of the comparator input voltage through a full conversion cycle. During the zero phase, all capacitors are shorted to V_{DD} through SW_{zero}. In the sample phase, the two DACs are connected in series through SW_{series} and DAC2 is referenced to V_{DD}. For an input range of $2V_{DD}$, the comparator inputs vary from $V_{DD}/2$ (when the input is 0V) to $3V_{DD}/2$ (when the input is $2V_{DD}$). This allows for a maximum of ± 0.45V on each DAC without reducing the LSB size. Compared to an ADC that requires a voltage divider to scale down the input voltage, this technique provides $2\times$ larger signals at the comparator inputs. When the sample phase terminates, the two DACs are disconnected from one another. At the same time, DAC1's MSB array and DAC2's Main array will be connected to GND. This places the common mode between the DACs at $V_{DD}/2$ and ensures that the comparator input voltage range stays within V_{DD}. At this point, all the bits will resolve as if the ADC is a differential ADC, unlike [10]. The common mode is constant at $V_{DD}/2$ during comparison steps, thus, simplifying the comparator design operating off a V_{DD} supply.

The extended algorithm also reduces the energy required by using a reference value of half the input range compared to a reference equal to the full input range in a conventional single-ended design. Since the energy is proportional to V_{ref}^2, DAC energy reduces by a factor of four. However, since two DACs are necessary, overall energy reduces by a factor of two.

Care must be taken on how V_{ref} is generated to really get these energy savings. As shown in [6], the energy for a

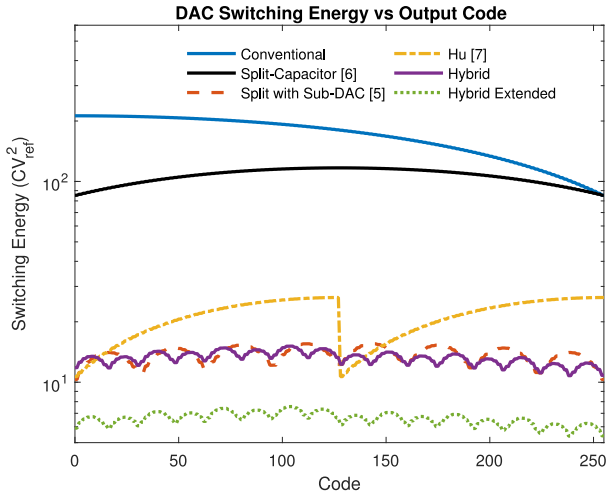

Fig. 4. DAC switching energy comparison for an 8b single-ended ADC.

TABLE I
MEAN ENERGY, NUMBER OF UNIT CAPACITORS, AND ENERGY-AREA PRODUCT (EAP) FOR DIFFERENT SWITCHING ALGORITHM

	Conventional	Split-Capacitor [6]	Hu [7]	Yip [5]	Hybrid	Hybrid Extended
Mean energy (CV^2)	169.67	106.17	21.08	13.67	13.18	6.59
# of C	128	128	256	48	32	64
EAP	21717.76	13589.76	5396.48	656.16	421.76	421.76

transition is given by Eq. (1):

$$E_{transition} = \int i_{ref}(t) V_{ref} dt \propto \alpha C V_{ref}^2 \quad (1)$$

where α is a factor based on the exact transition and C is the value of a unit capacitor in the array. This equation shows that the quadratic relationship of V^2_{ref} is linked to two key factors: the voltage level of V_{ref} and the total current drawn from V_{ref}, i.e., the quantity of charge (Q). No matter how V_{ref} is generated, the current level will scale with the value of V_{ref} as less charge will move in the capacitive DAC. However, if V_{ref} is generated by a lossy mechanism, such as an LDO, the value of the input voltage source must be used to calculate the effective energy requirement.

Generally speaking this method will always be more energy efficient than stepping up V_{DD} to sample inputs higher than V_{DD}. However, before using this method for the strict purpose of saving energy, a detailed analysis should be done to determine its worthiness at the system level.

C. Switching Energy

Figure 4 compares DAC switching energy for six different approaches with the same single-ended input range. Mean energy for a uniformly distributed input signal, number of unit capacitors, and EAP for these approaches are tabulated in Table I.

As described earlier, the hybrid DAC requires 3.5% less energy and 33% less capacitor area compared to [5]. When two hybrid DACs are combined to implement a hybrid extended-range architecture, the energy required is halved, but the number of capacitors doubles. In both cases, the proposed designs procures 35.72% lower energy-area product (EAP) compared to the next best algorithm. Moreover, the switching energy of the proposed design is less than one third of a prior extended-range 8b single-ended SAR ADC design [7]. If the proposed hybrid algorithm is used for differential inputs (not shown in Figure 4), switching energy only reduces by 3.5% compared to [5], but area reduces by 33% to yield the same improvement in EAP as the single-ended case.

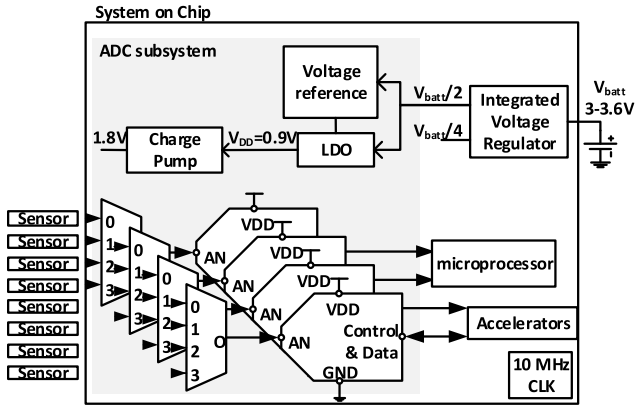

Fig. 5. ADC sub-system overview with supply independent 1.8 V single-ended input range.

As explained earlier, the energy savings associated with the extended-range architecture come from the lower voltage reference used ($V_{ref}/2$ vs. V_{ref} for an input range of V_{ref}). These savings will only fully materialize if the $V_{ref}/2$ is provided directly from a voltage source. If $V_{ref}/2$ is generated by lowering V_{ref} to $V_{ref}/2$ with an LDO, there won't be any energy benefit. In that case, the simple Hybrid DAC provides the best EAP. The extended-range algorithm is meant for systems where a supply-independent ADC input voltage range greater than the SoC supply is required, like in the RoboBee chip, or in systems where an efficient way to provide $V_{ref}/2$ exists (e.g., a switched-capacitor circuit).

III. IMPLEMENTATION

This section first provides an overview of the ADC system inside the Robobee "brain" SoC. Then, it describes the key design choices for the implementation of the three main building blocks in Figure 2: the comparator, DAC, and SAR logic.

A. ADC Subsystem Inside the SoC

Figure 5 provides an overview of the ADC subsystem embedded within the Robobee "brain" SoC comprising four independent ADC cores that accept up to 16 analog inputs via four 4:1 analog multiplexers. An integrated voltage reference and LDO circuitry create a process, voltage, temperature (PVT) independent 0.9V V_{DD} supply from a $V_{batt}/2$ supply provided by an integrated voltage regulator in the SoC [2]. An on-chip charge pump doubles the V_{DD} input to bootstrap necessary switches and provide reliable input sensing up to 1.8 V. Finally, a 10MHz fixed-frequency clock source within

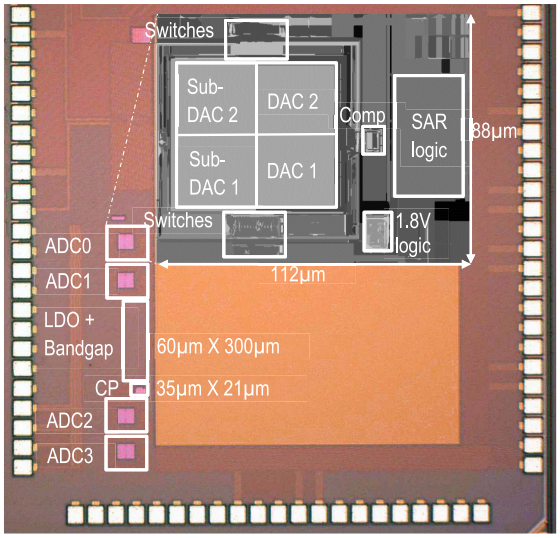

Fig. 6. Micrograph of the test chip in 40 nm CMOS. All ADC cores are shown with the charge pump (CP), LDO, and bandgap required in the application. The ADC core layout overlay shows ADC components.

the SoC sets the ADC clock, which imposes a maximum sampling rate of 1 MS/s per ADC since each conversion takes 10 steps. The proposed ADC can dynamically adjust the sampling time from 100 ns to 800 ns in order to accommodate different sensor output impedances. Consequently, the sampling rate reduces to 588.2 kS/s for the 800 ns sampling time.

B. ADC Implementation

Figure 6 shows a partial die photo of the "brain" SoC fabricated in TSMC's 40G CMOS process. The magnification of a single ADC core provides better view of the different blocks in the core. The proposed ADC core occupies 0.00986 mm^2 without the 4:1 analog multiplexers. The capacitor arrays use 44fF metal-oxide-metal (MOM) unit capacitors for a total equivalent input capacitance of 352fF. This can be reduced for 8b resolution. It was sized for a 10b implementation and wasn't scaled down once the SoC requirements changed from 10b to 8b due to negligible impact at the system level. The complete ADC subsystem—including four ADC channels multiplexed to 13 input pads, an LDO, bandgap, and charge pump (CP)—occupies 0.0655mm^2 as shown in the chip micrograph (Figure 7). The CP's area (735 μm^2) is the only overhead required to accommodate the extended 0 to 1.8 V input range for all four ADC cores.

The proposed hybrid extended-range design uses a StrongArm latch comparator (Comp) built using low-voltage, thin-oxide devices as shown on Figure 7. This is possible because during the sampling phase, CLK is held low to force $Q_{2,3}$ drain and source to V_{DD} and the voltage on the gate of $Q_{2,3}$ is comprised between $V_{DD}/2$ and $3V_{DD}/2$ (Figure 3). Consequently, $|V_{GD,GS}|$ of $Q_{2,3}$ never exceeds a value of $V_{DD}/2$. As the common mode during comparison stages sits at $V_{DD}/2$, plenty of headroom is available to design the comparator. By comparison, comparators in [7] and [10] would require thick-oxide input devices in our 40nm process to tolerate input voltages up to $2V_{DD}$ and both comparators must have rail-to-rail input range.

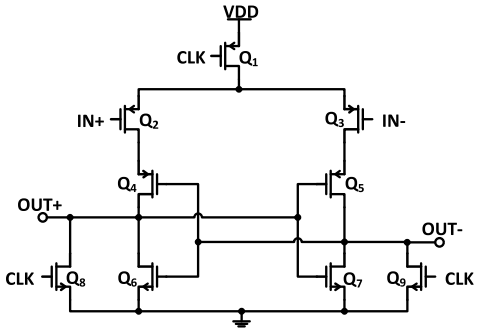

Fig. 7. Implementation of the StrongArm latch comparator.

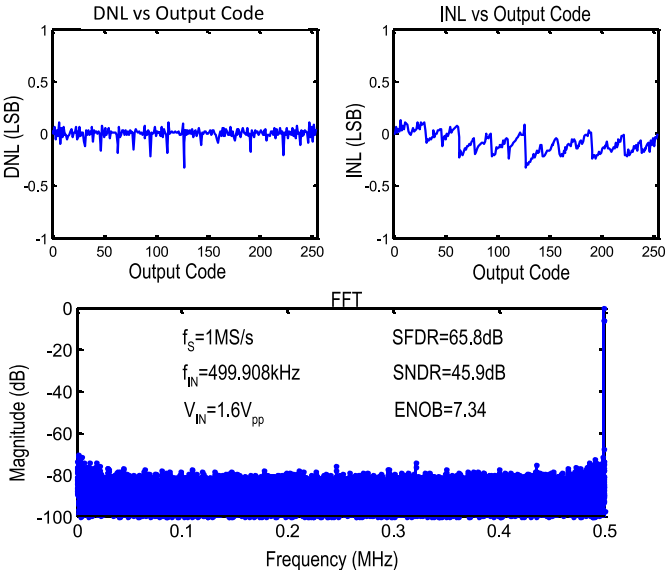

Fig. 8. Measurements results from 1 of the 24 channels from six chips measured all with close to average performance.

The 40G process, standard cells, and digital design flow chosen for the SoC unfortunately led to high leakage and dynamic power for the SAR logic. Nevertheless, we did not seek to further optimize the ADC's digital power given that the four ADC channels operating at 1MS/s account for less than 1% of the SoC's overall power budget. There is room to significantly reduce SAR logic power by using a low-power, low-leakage process flavor (e.g., 40LP), a low-power, low-leakage standard cell library, and/or reduce the supply voltage for the digital logic as in [5]. Based on simulations, the typical power breakdown for a single channel that consumes 16.1µW is: 87% SAR logic, 10% DAC, 1% comparator, and 2% 1.8V logic. Moreover, the simulated leakage accounts for 46% of the total power.

IV. Results

Figure 8 shows typical results measured across multiple test chip. The results from 24 ADC cores measured across six chips, powered by an external 0.9V supply, are consistent with one another. The average DNL across all 24 cores from six measured chips is 0.48LSB. While the average INL across all measured ADC cores is 0.50LSB, INL consistently increases from an average of 0.39LSB for ADC0 to an average

TABLE II
PERFORMANCE COMPARISON TO STATE-OF-THE-ART ADCS

	[3]	[4]	[5]	[7]	[10]	This Work
Technology	65nm	40nm	65nm	0.18 μm	0.18 μm	40nm
Resolution	10b	10b	8b	8b	9b	8b
Area (mm^2)	0.0258	0.0065	0.212	0.06	-	0.00986
Unit cap. (fF)	-	1.5	65	27	-	44
# cap 8b ADC	-	314*	92+4Cc	256	-	62+2Cc
Supply (V)	1.0	0.45	0.6	1.1	0.45	0.9
Input range	$\pm V_{DD}$	$\pm V_{DD}$	$\pm V_{DD}$	$1.09*V_{DD}$	$2*V_{DD}$	$2*V_{DD}$
Input type	Differential	Differential	Differential	Single-ended	Single-ended	Single-ended
DNL (LSB)	0.5	0.44	0.51	0.28	<0.5	0.48
INL(LSB)	2.2	0.45	0.43	0.81	<1	0.5
Sample rate (S/s)	1M	200k	100k	2k	200k	1M
Power (μW)	1.9	0.084	0.146	0.027	0.94	29.7 (11.0)
ENOB (bits)	8.75	8.95	7.51	7.4	8.27	7.29
FOM (fJ/c.-s.)	4.42	0.85	40.0	79.9	22	189.6 (70.2)

of 0.58LSB for ADC3, possibly because device matching degrades towards the chip's corner. At 1MS/s with 0.9V V_{DD}, the average SFDR, SNDR, and ENOB are 63.56dB, 45.64dB, and 7.29bits for a 499.908 kHz 1.6 Vpp input sine wave. When powered by the internal LDO, the only significant difference is the average INL degrades to 0.57LSB from 0.50LSB when powered off of an external 0.9V supply.

The average power measured for a single channel at 1MS/s is 29.7μW. However, power measurements across the six measured chips are inconsistent due to a +22% to -20% variation in leakage power. In contrast, measured dynamic power is consistent and only varies by +2.8% to -3.7%. These measurements agree with the ADC extracted corner simulations. On average, leakage accounts for 61% of the total ADC power measured. The power without leakage is 11μW and dominated at 77% by the SAR logic. The average FOM with and without leakage are 189.6fJ/conversion-step and 70.2 fJ/conversion-step. These numbers include overhead power from the charge pump. The charge pump's measured average power of 2.37μW is the only power overhead required to accommodate the extended 0 to 1.8V input range for all four ADC cores operating at 1MS/s. Table II presents a performance summary of the proposed hybrid extended-range design with comparisons to other relevant SAR ADCs.

V. CONCLUSION

A SAR ADC using two techniques to improve EAP and provide analog input range higher than the supply voltage has been presented. The hybrid split-capacitor sub-DAC technique allows reduction of the DAC area while also reducing energy. The extended-range algorithm allows $2V_{DD}$ analog input range with a small charge pump as the only overhead to bias input transistors. Four ADC cores have been built in each Robobee "brain" SoC fabricated in a 40nm CMOS process. A single ADC uses 0.00986mm^2 and consumes 29.4μW at 1MS/s powered by a 0.9V supply with a 499.908kHz $1.6V_{pp}$ input signal. High leakage power and dynamic power in the SAR controller significantly increases the power numbers reported in this brief. The FOM of this brief including controller leakage is 189.6 fJ/conversion-step while without leakage it is 70.2 fJ/conversion-step. Finally, there is room to improve the FOM by using a low-power digital library, resizing the DAC capacitors and modifying the algorithm to make the results in Figure 4 fully symmetric around the center code.

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