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A 7.5 GS/s flash ADC and a 10.24 GS/s time-interleaved ADC for backplane receivers in 65 nm CMOS

Hayun Chung[1] · Zeynep Toprak Deniz[2] · Alexander Rylyakov[3] · John Bulzacchelli[2] · Daniel Friedman[2] · Gu-Yeon Wei[4]

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Abstract This paper presents a 7.5 GS/s, 4.5 bit flash analog-to-digital converter (ADC) for high-speed backplane communication. A two-stage track-and-hold (T/H) structure enables high input bandwidth and low power consumption at the same time. A sampling clock duty cycle control technique, which allocates more tracking time to the bandwidth-limited second T/H stage, facilitates high sampling rates. A digital offset correction scheme compensates both random and systematic offsets due to process variation and T/H amplifier gain nonlinearity, simultaneously. Two test-chip prototypes were fabricated in a 65 nm CMOS process. Experimental results of a standalone ADC chip demonstrate 3.8 effective number of bits (ENOB) at 7.5 GS/s. The figure-of-merit (FOM) of the standalone ADC is 0.49 pJ/conversion-step. The second test chip combines two ADCs together in order to demonstrate a time-interleaved ADC (TI-ADC) for use in high-speed backplane receivers. The TI-ADC operates at 10.24 GS/s while achieving 3.5 ENOB and 0.65 pJ/conversion-step FOM.

Keywords High-speed · Analog-to-digital converter · Two-stage track-and-hold amplifier · Duty-cycle control · Backplane receiver

✉ Hayun Chung
hcchung@korea.ac.kr

[1] Korea University, Sejong, South Korea

[2] IBM T.J. Watson Research Center, Yorktown Heights, NY, USA

[3] Coriant Advanced Technology Group, New York, NY, USA

[4] School of Engineering and Applied Sciences, Harvard University, Cambridge, MA, USA

1 Introduction

As demand for high data rate communication continues to increase, high-speed backplane receivers require increasingly sophisticated equalization to compensate for channel imperfections and bandwidth limitations. In recent years, to fully benefit from advanced digital signal processing techniques, high-speed backplane receivers that utilize high-speed front-end analog-to-digital converters (ADCs) followed by digital equalizers have been proposed [1, 2].

The benefits of such ADC-based receivers are (1) portability and design reusability, as digital circuits can be easily reconfigured depending on channel environments; (2) good process scalability, as digital circuits scale well with fabrication process; (3) capability to implement feed-forward equalization (FFE), as digitized input signals are easily stored and delayed unlike analog signals; and (4) immunity to on-die parameter variations and noise, as digital circuits are more robust to on-die nonidealities.

However, designing front-end ADCs for such receivers is not trivial [3–12]. The ADCs require high input bandwidth while operating at high sampling rates in order to support high input data rates. Low power consumption is also critical to meet the tight power budgets of high-speed backplane transceivers. In [13], Yang et al. suggest maintaining the front-end ADC's figure-of-merit (FOM) below 0.5 pJ/conversion-step for reasonable total I/O power consumption. Although this FOM is possible for low sampling rate ADCs, high sampling rate ADCs suffer from bandwidth limitations associated with the input track-and-hold (T/H) stage [3, 4, 7]. This paper describes a two-stage T/H topology with duty-cycle control of the sampling clock, which enables high-speed operation while achieving a low FOM. Moreover, the high input bandwidth of the proposed ADC facilitates time-interleaving multiple ADCs

together (TI-ADCs) that offer even higher data rates, making them applicable to backplane receivers.

The remainder of this paper is organized as follows. Section 2 provides an overall description of the proposed ADC architecture with emphasis on how the proposed two-stage T/H input stage and duty cycle adjustment of the sampling clock together improve bandwidth. Section 3 then describes the circuit designs for key components of the ADC. Finally, Sect. 4 presents experimental results from two test-chip prototypes—a standalone ADC and a two-way time-interleaved ADC—to verify low FOM and high-speed operation.

2 Architecture

This paper presents a 4.5 bit, 6–7.5 GS/s front-end ADC for ADC-based receivers. Combining a pair of ADCs together and interleaving them in time makes the design attractive for high data rate backplane receivers operating at 12–15 Gbps. This section first focuses on the ADC architecture and describes two key innovations that improve input bandwidth and sampling rate.

2.1 Overall ADC architecture

Figure 1 shows the proposed ADC architecture, which implements a flash-type structure typically chosen to enable high sampling rates. A two-stage track-and-hold (T/H) circuit at the front-end minimizes input capacitance of the first stage. The second stage drives 22 1-bit comparators that digitize the input analog signal and generate a 4.5-bit output. The two-stage topology also buffers the sensitive sampling node in the first stage from coupling noise at the output of the second stage. A clock duty cycle controller allocates more tracking time to heavily loaded second stage to further improve the sampling rate. A reference generator taps out differential reference voltages from a resistor ladder for each comparator. A digital offset calibration block tunes the individual reference levels to compensate random and systematic offsets associated with both the front-end T/H and comparators.

2.2 Two-stage T/H with sampling clock duty cycle control

Designing T/Hs with high input bandwidth and high sampling rate can be challenging [3, 4, 7]. As the T/H output node suffers from large capacitive loading caused by multiple comparators, a large buffer is required to successfully track the high-speed input signal and achieve high sampling rate. However, the large buffer adds a large capacitive loading at the high-speed input node leading to input bandwidth limitation, and vice versa. While buffering up the T/H output can decoupling the high-speed input node from the heavily loaded output node, heavy capacitive loading at the output may require multiple buffer stages leading to high power consumption. We propose a two-stage T/H with duty cycle control to achieve high input bandwidth and high sampling rate while maintaining low power consumption. [14]. Figure 2 shows a conceptual block diagram of the proposed two-stage T/H and the sampling clock duty cycle controller. Each stage consists of a sampling switch driven by complementary clocks, a small hold capacitor, and a unity gain buffer. The large capacitive loading due to multiple comparators (i.e., C_{comp}) is also shown at the T/H output. Figure 3(a) illustrates the two-stage T/H operation via three waveforms that represent (i) the input, (ii) the first stage sampler output, and (iii) the T/H output signal. Notice that while the first stage must track the high-frequency input signal, the second stage only tracks a settled voltage held and driven by the first stage. Since, the second stage only needs to reach the settled DC voltage within the tracking time, a small buffer can be employed in the first stage T/H. Downsizing the unity-gain

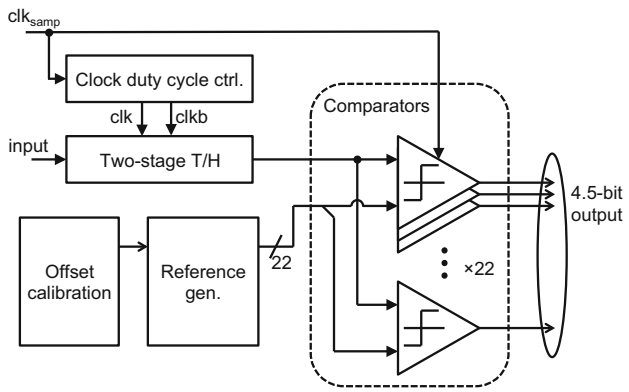

Fig. 1 Overall ADC architecture

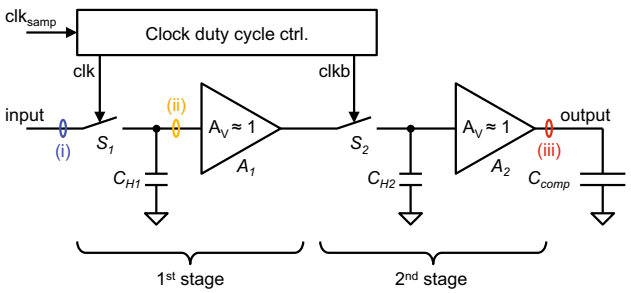

Fig. 2 Block diagram of the proposed two-stage T/H with sampling clock duty cycle control

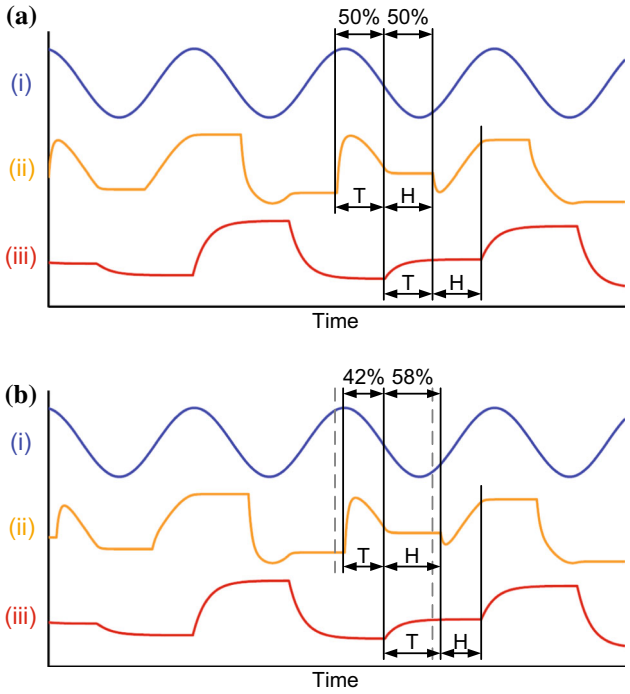

Fig. 3 Timing diagrams of the proposed two-stage T/H **a** without and **b** with sampling clock duty cycle control

buffer in the first stage T/H maximizes input bandwidth while also reducing power consumption.

Although the two-stage T/H structure can significantly improve T/H input bandwidth, heavy capacitive loading on the T/H output can still limit the sampling rate. One solution is to size up the second stage buffer (i.e., A_2), but this affects the design of the first stage (a larger A_1 buffer), degrading input bandwidth and increasing power consumption. This bandwidth degradation is especially undesirable for designs that time-interleave multiple ADCs to further increase aggregate data rates. Instead, we propose to allocate uneven tracking times to the first and second T/H stages. Figure 3(b) illustrates the proposed sampling clock duty cycle control technique. Allocating more tracking time within a clock cycle to the second stage allows more time for the second stage to drive the large capacitive load imposed by the comparators, while preserving high bandwidth and low power advantages of the first stage. Shortening the sampling clock duty cycle by 8 % extends tracking time of the second T/H stage by 16 % and improves the overall sampling rate by 16 %. Simulation results show that the two-stage T/H and the sampling clock duty cycle controller each consume 8 % of the overall ADC power consumption. Embedding the sampling clock duty cycle controller within the clock distribution network can further reduce power consumption.

3 Circuit design

3.1 Two-stage T/H with clock duty cycle control

Figure 4 presents the CMOS circuit implementation of the proposed differential two-stage T/H ADC front-end, where each stage consists of a pair of pMOS sampling switches followed by a differential amplifier. Since the input common-mode voltage is high (i.e., 0.8 V) and the voltage swing of each differential input is small (i.e., 0.4 V_{pk-pk}), only pMOS transistors are needed for the differential sampling switches. To minimize pedestal error caused by charge injection from the MOS sampling switches, dummy transistors are added in next to the switches, except for the differential inputs, which are low impedance nodes. Small cross-coupled capacitors connected across the differential amplifiers, relying on a few femtofarads of wire parasitics, reduce glitching at the amplifier output due to C_{gd} of the amplifier input devices. Figure 4 does not show explicit hold capacitors because the small parasitic capacitances of the wire and amplifier input devices suffice for high sampling rates.

Figure 5 shows the circuit implementation of the sampling clock duty cycle controller. To modify the duty cycle of the input clock, the controller tunes rise/fall times of the differential clocks by adjusting effective P/N ratio of the clock buffers using a 2-bit thermometer control code. Weak cross-coupled inverters, added to every inverter stage, help align the differential clock edges. Simulation results show that the 2-bit thermometer control can shorten clock duty cycle from 50 % down to 42 % extending the tracking time of the second T/H stage by 13 ps at 6.25 GHz. Although the additional delay cells in the duty cycle controller increase power consumption and jitter on the sampling clock, the controller can be included within the clock distribution network to avoid such penalties.

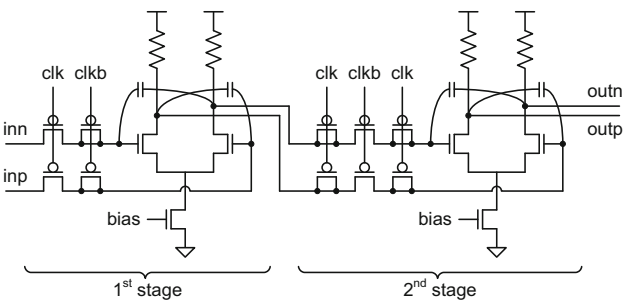

Fig. 4 Two-stage T/H circuit implementation

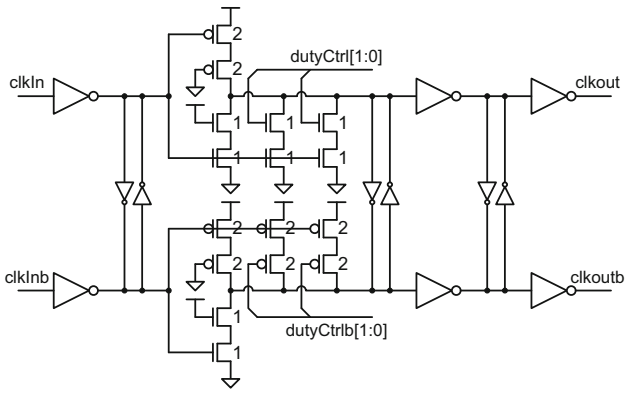

Fig. 5 Clock duty cycle controller circuit

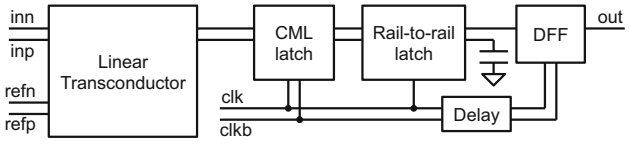

Fig. 6 Block diagram of a 1-bit comparator

3.2 Comparator with offset calibration

Figures 6 and 7 illustrate the block diagram of a 1-bit differential comparator and circuit implementations of its building blocks, respectively. Each 1-bit comparator consists of a linear transconductor followed by two stages of latches and a flip-flop. The linear transconductor [1] compares the differential inputs (inn and inp) against differential reference levels (refn and refp) to make a 1-bit decision. To minimize parasitic capacitance of all 22 comparators, which can limit T/H bandwidth, the linear transconductor employs minimum size devices. Moreover, the linear transconductor was chosen to buffer the T/H output from potentially large clock feedthrough from multiple comparators firing simultaneously. Two high gain latches [i.e., a current mode logic (CML) latch and a rail-to-rail latch] and a D flip-flop mitigate metastability and generate a full-swing, single-ended output.

One drawback of using minimum size input devices in the comparators is heightened susceptibility to on-die parameter variations, resulting in large input-referred offsets. The T/H amplifier gain nonlinearity further adds systematic offsets, as shown in Fig. 8. The solid grey line represents simulated T/H output voltages with respect to input voltages. The resulting T/H amplifier gain nonlinearity degrades towards the ends due to compression of the buffers. Rather than struggling to design out the observed deviation from the ideal linear relationship (dotted grey line), it is much simpler to compensate for this systematic

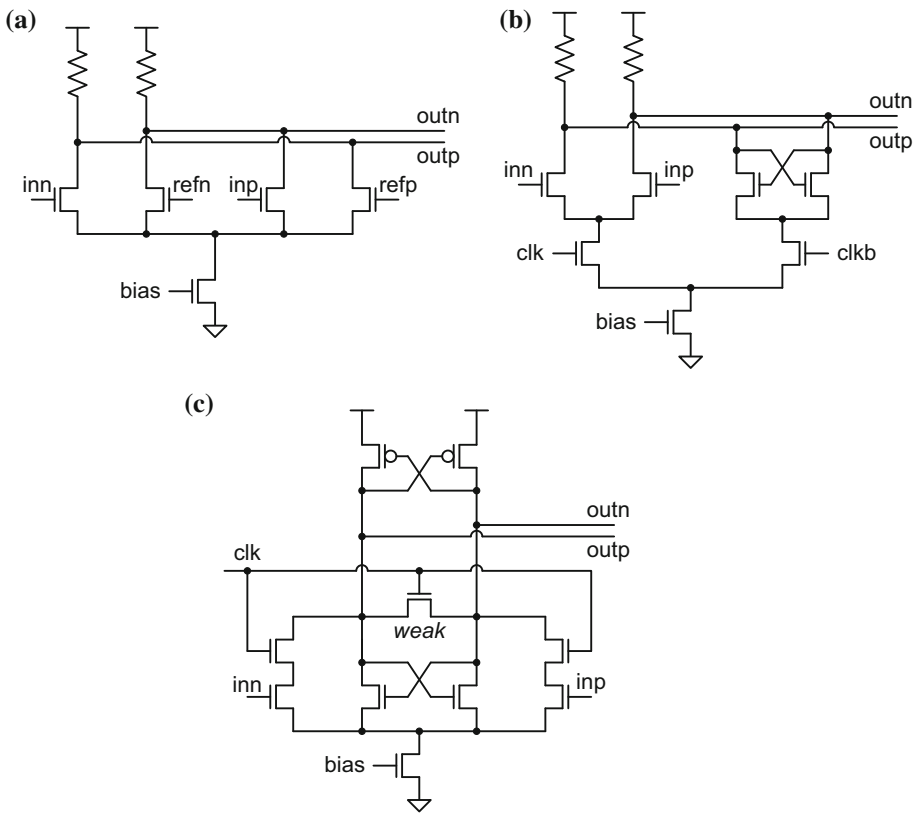

Fig. 7 Building blocks of a 1-bit comparator: **a** linear transconductor, **b** CML latch, and **c** rail-to-rail latch

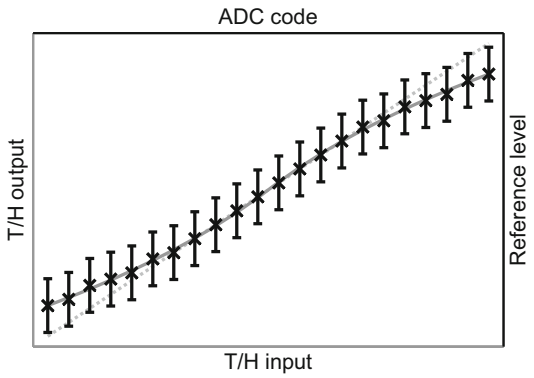

Fig. 8 T/H gain nonlinearity (*grey lines*) and comparator reference level connections (black bars and X's)

offset using a digital offset calibration circuit already required to deal with random offsets in each comparator.

We implemented a digital calibration scheme that employs a reference select circuit [15] shown in Fig. 9. This circuit allows fine-grained adjustment of reference voltages that feed each of the 22 comparators to compensate for offsets. Again, the high common-mode voltage (i.e., 0.8 V) allows for a simple pMOS based 8:1 multiplexer that covers ±1.75 least significant bits (LSBs) in 0.5 LSB steps. This range was chosen to cover a majority of the offset found via simulation. The T/H amplifier gain nonlinearity determines the median reference voltage for each comparator. Referring back to Fig. 8, the X's correspond to median voltage levels for each of the comparator references to account for systematic T/H amplifier gain nonlinearity. The black bars illustrate the calibration range. Finally, the digital calibration scheme also includes a static comparator reassignment technique [16] to constrain the size of the reference select circuit, but still compensate for worst-case offsets that extend beyond the calibration range.

4 Experimental results

To evaluate the performance of the proposed ADC, two test-chip prototypes were implemented—(1) a standalone ADC chip to measure ADC-only performance and (2) a two-way TI-ADC chip to verify ADC performance when used for high-speed backplane receiver applications, which often employ time-interleaved architectures to achieve higher sampling rates. Both test chips were fabricated in a 65 nm CMOS process.

4.1 Standalone ADC

Figure 10 shows a die photograph of the standalone ADC chip, which consists of a core ADC and a serial interface. The combination of a two-stage T/H, clock duty cycle control technique, and digital offset calibration enables the ADC to utilize small size transistors, significantly reducing the core area. As a result, the ADC core area occupies only 0.01 mm^2.

Figure 11 illustrates a simplified block diagram of the test setup used to measure the standalone ADC. Raw 22 thermometer-coded comparator outputs—before thermometer-to-binary code conversion—are used for analysis. To avoid a large number of pins, the test chip was designed to only drive out three comparator outputs at a time using three on-chip 8:1 multiplexers. Perfect synchronization between the clock and input signals allows reconstruction of the full ADC output by combining results from eight separate runs of the same experiment. Unfortunately, stabilizing the timing between two high-frequency signal generators proved difficult even with improved synchronization utilizing a 10 MHz rubidium source. A slow phase drift between the input and clock signals led to a significant amount of errors when comparator outputs measured at different times were combined together to reconstruct the full ADC output. To work around this phase drift issue, we

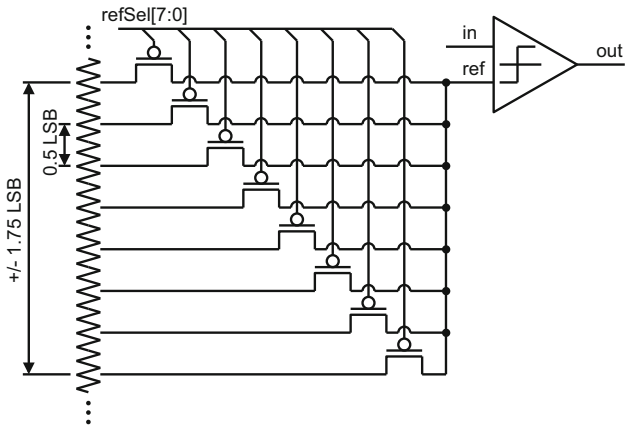

Fig. 9 Reference select circuit for digital offset calibration

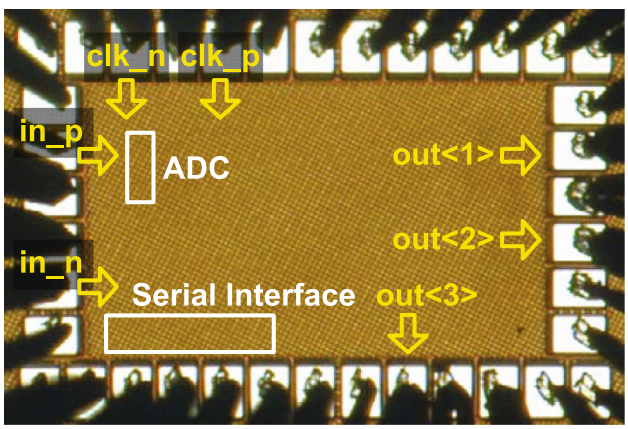

Fig. 10 Die photograph of the standalone ADC chip

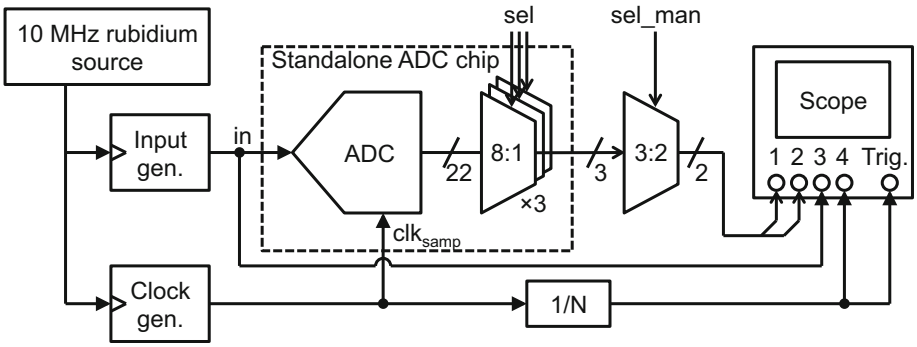

Fig. 11 Simplified test setup for the standalone ADC measurements

instead simultaneously measured two comparator outputs and the input signal, along with a divided down version of the ADC's sampling clock signal, which was used as the trigger signal for the oscilloscope. Then, multiple measurements of all comparator outputs were realigned with respect to the time difference between the input and trigger signals. Even with this realignment, the ADC performance reported in this section may be pessimistic due to imperfections (e.g., residual phase errors) in the test setup.

Figure 12 plots the measured ADC linearity before and after digital offset calibration. The comparator offsets are manually calibrated using the reference select circuit. Only random offsets due to device mismatch remain because the systematic offsets caused by T/H buffer nonlinearity was compensated prior to fabrication by pre-distorting the median of the reference level connections. When comparator offsets turned out to be larger than ±1.75 LSB, comparator reassignment takes care of comparators with offsets that extend beyond the calibration circuit's range. With offset calibration, the differential nonlinearity (DNL) and integral nonlinearity (INL) improve from 3.4 to 0.35 LSB and from 2.6 to 0.38 LSB, respectively.

To verify the advantages of sampling clock duty cycle control for the proposed two-stage T/H, ADC performance was measured across wide ranges of input frequencies and sampling rates. Figure 13(a) plots the signal-to-noise-and-distortion ratio (SNDR) of the proposed ADC across different sinusoidal input frequencies measured at 6 GS/s. Since the two-stage T/H structure enables high input bandwidth, the ADC achieves 25 dB SNDR up to 6 GHz input frequency. Figure 13(b) shows the SNDR across different sampling rates with Nyquist frequency inputs that cause large and frequent swings at the second T/H output. Consequently, Nyquist frequency inputs stress the second stage bandwidth limitation that degrades ADC sampling rate. As expected, with 50 % sampling clock duty cycle (i.e., *duty cycle ctrl.* = 00), SNDR degrades as sampling

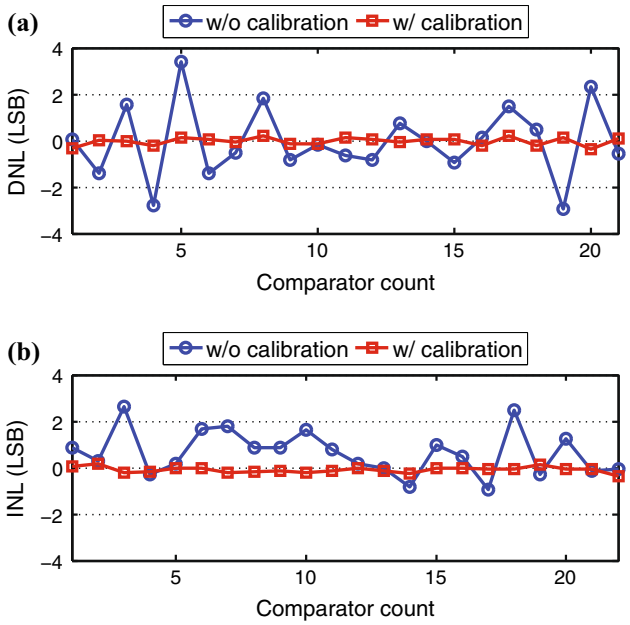

Fig. 12 Measured ADC linearity: **a** DNL and **b** INL

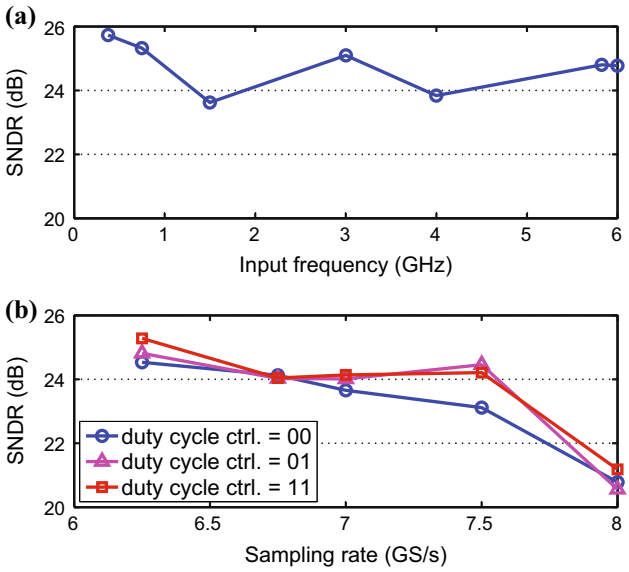

Fig. 13 Measured SNDR: **a** SNDR vs. f_{in} (f_s = 6 GS/s) and **b** SNDR vs. f_s (f_{in} = Nyquist frequency)

rate increases due to second stage T/H bandwidth limitations. Measurement results for the proposed sampling clock duty cycle control technique (i.e., *duty cycle ctrl.* = 01 and 11) verify that the proposed technique can improve ADC performance at high sampling rates by allowing more tracking time at the bandwidth-limited second T/H stage. At 7.5 GS/s, the SNDR improves by 1.3 dB, achieving 24.5 dB, which translates to 3.8 effective number of bits (ENOB). The power consumption at this operating point was only 52 mW from a 1 V supply, which translates to 0.49 pJ/conversion-step FOM.

Table 1 summarizes the performance of the standalone ADC and compares this work to state-of-the-art ADCs. Since this standalone ADC does not employ time-interleaving, the table only lists ADCs that also do not implement a time-interleaved architecture. As the two-stage T/H with duty cycle control significantly improves sampling rate, the proposed ADC achieves the highest sampling rate. Moreover, as the proposed two-stage T/H structure and minimum sized transistors in the comparators enable very high input bandwidth, the proposed ADC achieved effective resolution bandwidth higher than 6 GHz. This is more than $\times 2$ higher compared to the highest input frequencies reported in prior arts. Such high input bandwidth enables using this standalone ADC in a time-interleaved structure for high-speed backplane receivers discussed in the next section.

4.2 Two-way time-interleaved ADC

To emulate high-sampling-rate operation of a front-end ADC used in a high-speed backplane receiver, two identical standalone ADCs were time-interleaved (TI-ADC), operating off of alternating clock phases, and integrated together in a single chip. Figures 14 and 15 show the die photograph and block diagram of the two-way time-interleaved ADC test-chip prototype, respectively. Since reading out high-data-rate outputs from both ADCs in real-time

Table 1 Standalone ADC performance comparison

	This work	[3]	[4]	[5]
Architecture	Flash	Flash	Flash	Flash
Technology (nm)	65	65	180	32
Sampling rate (GS/s)	7.5	5	4	5
Max. input frequency (GHz)	6	2.5	1.3	2.5
Resolution (bits)	4.5	6	4	6
ENOB (bits)	3.8	5	3.4	4.8
FOM (pJ/conv.-step)	0.49	1.97	2.16	0.06
Power (mW)	52	320	89	8.5
Area (mm^2)	0.01	0.3	0.88	0.02

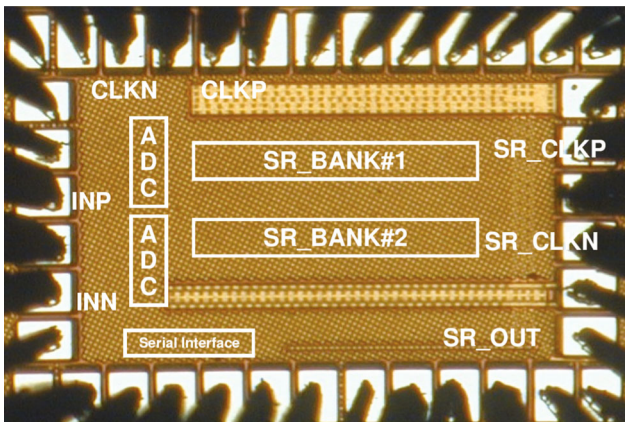

Fig. 14 Die photograph of the two-way time-interleaved ADC chip

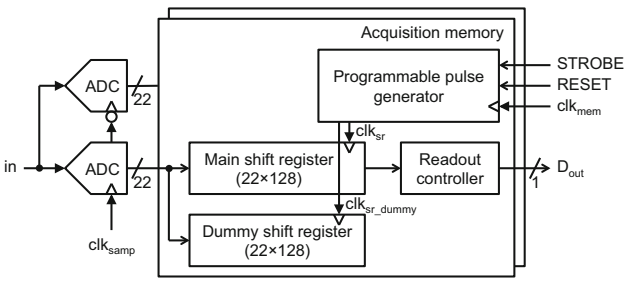

Fig. 15 Block diagram of the two-way time-interleaved ADC chip

is challenging, we implemented an on-chip acquisition memory. Once the high-speed ADC outputs are stored in the acquisition memory, they can be slowly read out using a serial interface (i.e., readout controller). As shown in Fig. 15, each of the two time-interleaved ADCs is connected to an acquisition memory that can store up to 128 samples. Therefore, the two time-interleaved acquisition memories can collectively save up to 256 consecutive samples. The operation of the on-chip acquisition memory is as follows. Lowering the *RESET* signal enables the main shift register by forwarding the clk_{mem} signal to the clock signal of the main shift register (i.e., clk_{sr}). Once enabled, the main shift register samples the ADC output and stores the value every clk_{sr} cycle. Since the memory depth is 128, the main shift register only keeps the most recent data sampled within 128 clk_{sr} cycles and discards all other data samples.

In order to evaluate performance of the TI-ADC as a front-end ADC of a backplane receiver, we had to collect ADC outputs over a long data sequence, much longer than 256 samples. To achieve this, we used a programmable-window data acquisition technique. Utilizing a *STROBE* signal (synchronized to the repeating input data pattern) and a programmable pulse generator, each acquisition memory stores ADC outputs over a specific time window.

As shown in Fig. 16, once the *STROBE* signal fires, the programmable pulse generator counts clk_{mem} cycles and disables the clk_{sr} signal after $(M + 1) \times 128$ cycles, where M corresponds to the programmed window number. Though the main shift register only keeps the most recent 128 data samples, the acquisition memory can save ADC outputs for long data sequences by incrementing M to collect data within any time window between $(M \times 128) + 1$ and $(M + 1) \times 128$ clk_{mem} cycles from assertion of the *STROBE* signal. Repeated measurements with the same input and *STROBE* signals and sweeping M (programmed with a serial interface) from 0 to 210 enable capturing 26,880 data samples. Since two acquisition memories are time-interleaved, as described in Fig. 15, up to 53,760 consecutive data samples can be acquired. Since abruptly disabling the clk_{sr} can result in *dI/dt* noise on the supply, the test chip includes a dummy shift register and forwards clk_{sr} to clk_{sr_dummy} when clk_{sr} is disabled.

In TI-ADCs, mismatches between the ADCs (e.g., gain mismatch and time skew) may degrade the overall ADC performance. While the comparator offset calibration circuits can handle the gain mismatch between the two time-interleaved ADCs, the time skew between the two differential sampling clocks, if not addressed, can affect the TI-ADC performance. Figure 17 shows the impact of time skew on the TI-ADC performance. Three simulated FFT plots with different skew conditions (i.e., no skew, 1-ps skew and 10-ps skew) based on an accurate behavioral ADC model presented in [17] are shown. The time skew introduces spurs at $\pm f_{in} \pm f_s/2$ (i.e., $\pm$ 4.95 $\pm$ 1024/2 = 0.17 and 10.07 GHz) which significantly degrades SNDR performance. Figure 18 presents the measured FFT at 10.24 GS/s with 4.95 GHz sinusoidal input. The spur at 0.17 GHz implies that a 9-ps of time skew exist between the two time-interleaved ADCs.

Performance of the TI-ADC was evaluated at 10.24 GS/s with a near-Nyquist frequency input (f_{in} = 4.95 GHz). The measured SNDR is 22.7 dB, which translates to 3.5 ENOB, and power consumption was 77 mW from a 1 V

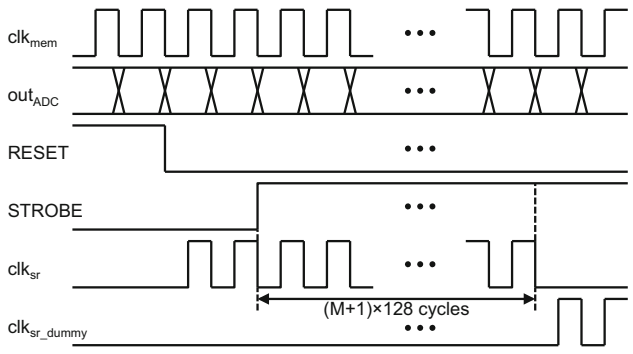

Fig. 16 Timing diagram of the proposed on-chip acquisition memory

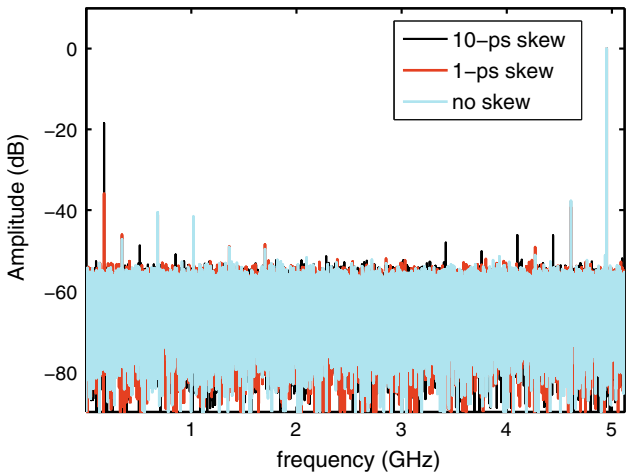

Fig. 17 Simulated FFT at 10.24 GS/s with 4.95 GHz sinusoidal input with different time skew conditions

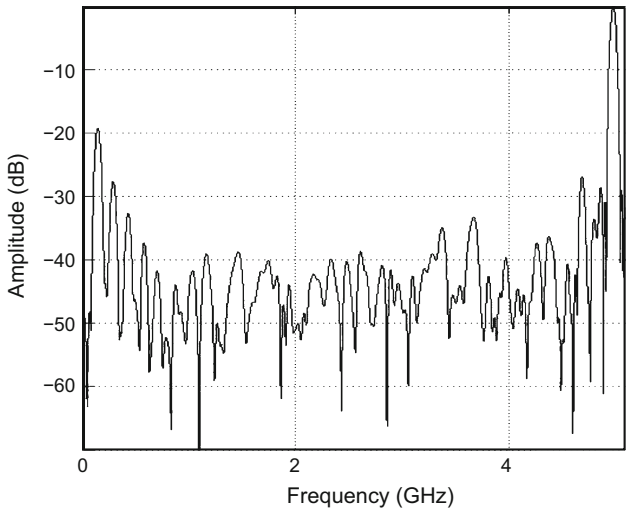

Fig. 18 Measured FFT at 10.24 GS/s with 4.95 GHz sinusoidal input

supply. The FOM at this operating point is 0.65 pJ/conversion-step. Table 2 compares performance of the proposed TI-ADC with prior published works that have sampling rate higher than 10 GS/s. The proposed TI-ADC occupies much smaller area, at least 10 times smaller than other designs. This is mainly because the proposed TI-ADC can implement two-way time-interleaving by relying on the high input bandwidth and high sampling rate of the standalone ADC. Lastly, the FOM and sampling rate are comparable to prior work.

To estimate the TI-ADC-based receiver's performance, a test setup with a PRBS input data sequence and a backplane channel was used, as shown in Fig. 19. A 10.24 GHz high-frequency clock source is used to generate the input data pattern and is divided by two to provide half-rate clocks for the receiver (i.e., TI-ADC chip). As discussed

Table 2 TI-ADC performance comparison

	This work	[6]	[7]	[8]	[9]	[10]
Architecture	Flash	Flash	Pipeline	Flash	Flash	SAR
TI depth	2	8	8	4	4	8
Technology (nm)	65	65	90	40	40	65
Resolution (bits)	4.5	5	6	6	6	6
ENOB (bits)	3.5	3.9	5.1	4.6	5.1	4.0
Sampling rate (GS/s)	10.24	12	10.3	10	10.3	10
Power (mW)	77	81	1600	139	240	79
FOM (pJ/conv.-step)	0.65	0.46	4.56	0.59	0.7	0.48
Area (mm^2)	0.02	0.44	N/A	0.35	0.27	0.52

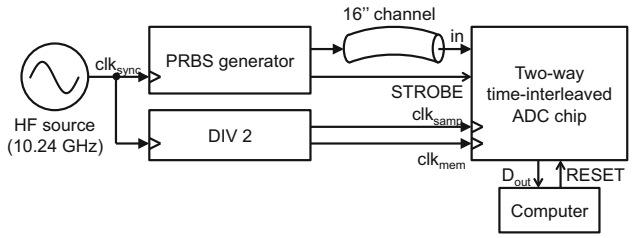

Fig. 19 Block diagram of the ADC-based receiver test setup

above, time skew between the two time-interleaved ADC sampling clocks degrades the ADC SNDR performance significantly. However, the impact of time skew on the receiver performance is relatively low, especially when there is sufficient timing margin, as the goal of receiver is in recovering the incoming data bits rather than correctly digitizing the incoming signal. Therefore, no extra circuits for time skew adjustment is employed. Figure 20 shows eye diagrams captured by the TI-ADC- based receiver test setup. Two channel scenarios, a coaxial cable and a 16″ backplane channel, were used to evaluate receiver performance with negligible and significant amounts of channel imperfections, respectively. While the eye diagram with a coaxial cable is wide open, the eye diagram with a 16″ backplane channel is completely closed due to channel bandwidth limitations and imperfections. In order to open the completely closed eye in Fig. 20(b), we post-processed the results using a receiver-side equalizer with 7-tap FFE and 13-tap DFE from [17]. Figure 21 shows eye diagrams before and after equalization. The open equalized eye diagram confirms that the accuracy of the proposed front-end TI-ADC is sufficient for a digital equalizer to reliably reconstruct the original input sequence. While more extensive discussions on equalizer configuration may reveal interesting features enabled by the ADC-based receivers, they are beyond the scope of this paper.

5 Conclusion

A 7.5 GS/s 4.5 bit flash ADC and a 10.24 GS/s two-way TI-ADC have been presented. The proposed two-stage T/H structure effectively decouples the input node that requires high bandwidth from the heavily loaded output node to

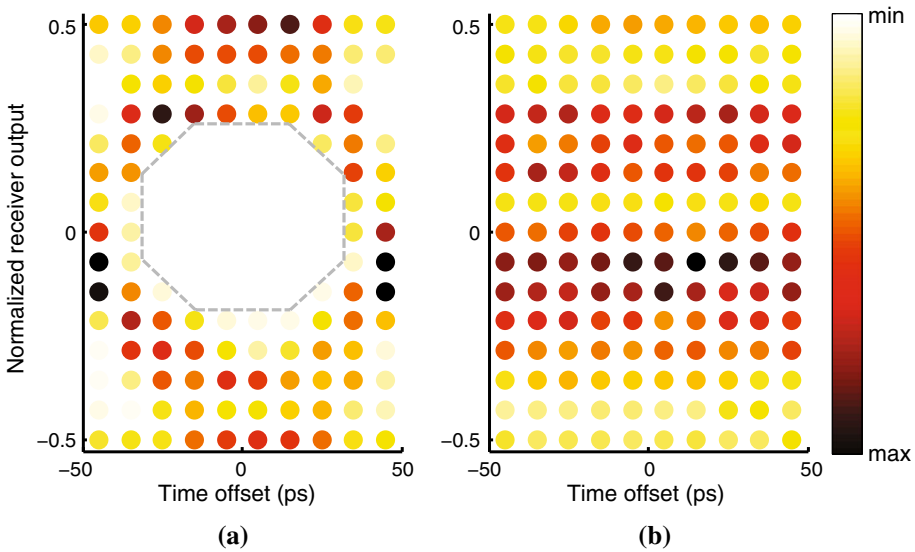

Fig. 20 Measured eye diagram at 10.24 Gbps transmitted over **a** a coaxial cable and **b** a 16″ backplane channel

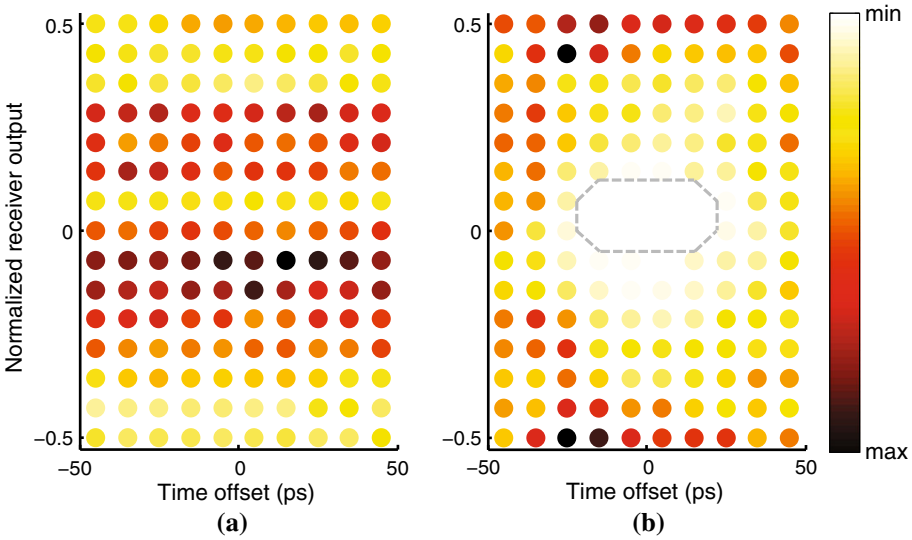

Fig. 21 Measured eye diagram at 10.24 Gbps with a 16″ backplane channel **a** before and **b** after equalization

achieve high input bandwidth with low power consumption. Furthermore, the sampling clock duty cycle control technique allocates more tracking time to the bandwidth-limited second T/H stage when the sampling rate is high. The combination of the two techniques reliably extends sampling rates without significant power penalties, simultaneously achieving high input bandwidth, high sampling rate, and low power consumption. The proposed digital offset calibration block not only compensates for random offsets due to on-die parameter variations, but also cancels out systematic offsets imposed by T/H nonlinearity.

Two test-chip prototypes were fabricated in a 65 nm CMOS process to evaluate the performance of a standalone ADC and that of a TI-ADC separately. Experimental results measured from the standalone ADC chip demonstrate that the proposed ADC with two-stage T/H and sampling clock duty cycle control achieves 3.8 ENOB at 7.5 GS/s while consuming only 52 mW, which translates to a 0.49 pJ/conversion-step FOM. The TI-ADC chip operating at 10.24 GS/s achieves a FOM of 0.65 pJ/conversion-step, which is comparable to prior work. The active area is only 0.02 mm^2, which is at least 10 times smaller than the previous works, as only two ADCs are time-interleaved. The experimental results with the ADC-based receiver test setup confirm that the TI-ADC successfully quantizes an input data sequence and post processing via a digital equalizer recovers the original input sequence.

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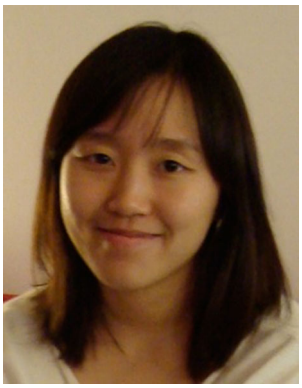
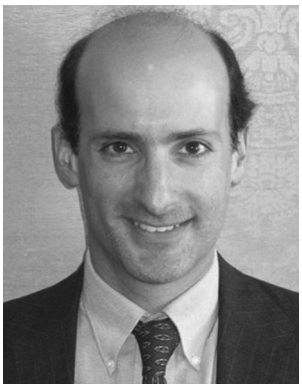


Hayun Chung Hayun Chung is an Assistant Professor of Electronic and Information Engineering at Korea University, South Korea. She received her B.S. and M.S. degrees in Electrical Engineering from Seoul National University in 2002 and 2004, respectively, and Ph.D. degree in Engineering Sciences from Harvard University in 2009. From 2009 to 2011 she was with Keio University as a Research Associate. Her research interest includes variability-aware re-configurable circuit designs, digitally assisted analog circuits and inductive-coupling interfaces.

Zeynep Toprak-Deniz Zeynep Toprak-Deniz received the B.S. degree from Istanbul Technical University, Istanbul, Turkey, the M.S. degree from Sabanci University, Istanbul, Turkey, and the Ph.D. degree from the Swiss Federal Institute of Technology, Lausanne (EPFL), in 1999, 2001, and 2006, respectively, all in electrical engineering. From 1999 to 2003, she worked at ST Microelectronics (formerly Alcatel Microelectronics R&D) on various projects including DC–DC converters, VCXOs, and low-jitter PLL-based Clock and Data Recovery (CDR) circuits. In January 2003, she joined EPFL as a graduate student, working in the Microelectronic Systems Laboratory as a research assistant. In her doctoral work, she designed and demonstrated a unique analog computation system for global energy management and optimization in Net- work-on-Chip applications. In 2007, she joined the IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, as a Research Staff Member. Her research interests include the design of mixed-signal CMOS circuits for high-speed data communications, power-efficient and high-speed analog-to-digital converters, and voltage regulators. She holds five U.S. patents.

Alexander Rylyakov Alexander Rylyakov received the M.S. degree in physics from the Moscow Institute of Physics and Technology, Moscow, Russia, in 1989, and the Ph.D. degree in physics from the State University of New York (SUNY) at Stony Brook, NY, USA, in 1997. From 1994 to 1999 he worked in the Department of Physics at SUNY Stony Brook on the design and testing of integrated circuits based on Josephson junctions. From 1999 to 2015 he worked in IBM T. J. Watson Research Center as a research staff member. His main current research interests are in the areas of digital phase-locked loops and integrated circuits for wireline and optical communication. In 2015, he joined Coriant Advanced Technology Group as a senior mixed signal design engineer.

John F. Bulzacchelli John F. Bulzacchelli received the S.B., S.M., and Ph.D. degrees in electrical engineering, all from the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 1990, 1990, and 2003, respectively. From 1988 to 1990, he was a co-op student at Analog Devices, Wilmington, MA, USA, where he invented a new type of delay-and-phase-locked loop for high-speed clock recovery. From 1992 to 2002, he conducted his doctoral research at the IBM T.J. Watson Research Center, Yorktown Heights, NY, USA, in a joint study program between IBM and MIT. In his doctoral work, he designed and demonstrated a superconducting bandpass delta-sigma modulator for direct A/D conversion of multi-GHz RF signals. In 2003, he became a Research Staff Member at this same IBM location, where his primary job is the design of mixed-signal CMOS circuits for high-speed data communications. He has also been investigating new architectures and circuits for high-performance integrated voltage regulators. Dr. Bulzacchelli received the Jack Kilby Award for Outstanding Student Paper at the 2002 IEEE International Solid-State Circuits Conference (ISSCC), was a co-recipient of the Beatrice Winner Award for Editorial Excellence at the 2009 ISSCC, co-authored the IEEE JOURNAL OF SOLID-STATE CIRCUITS article awarded Best Paper of 2009, and was a co-recipient of the 2011 IEEE Custom Integrated Circuits Conference (CICC) Best Regular Paper Award. He holds 29 U.S. patents.



Daniel J. Friedman Daniel J. Friedman received the Ph.D. degree in engineering science from Harvard University, Cambridge, MA, USA, in 1992. After completing consulting work at MIT Lincoln Labs and postdoctoral work at Harvard in image sensor design, he joined the IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, in 1994. His initial work at IBM was the design of analog circuits and air interface protocols for field-powered RFID tags. In 1999, he joined the mixed-signal communications IC design group and turned his attention to analog circuit design for high-speed serializer/deserializer macros. He managed the mixed-signal team from 2000 to 2009, focusing efforts on serial data communication and clock synthesis applications. In 2009, he became manager of the communication circuits and systems group, adding responsibility for teams in millimeter-wave wireless and digital communications IC design. He has authored or co-authored more than 40 technical papers in circuit topics including serial links, PLLs, RFID, and imagers. He holds more than 50 patents. His current research interests include high-speed I/O design, PLL design, and circuit/system approaches to enabling new computing paradigms. Dr. Friedman was a co-recipient of the Beatrice Winner Award for Editorial Excellence at the 2009 ISSCC and the 2009 JSSC Best Paper Award given in 2011. He has been a member of the ISSCC International Technical Program Committee since 2008. He has served as the Wireline sub-committee chair for ISSCC since 2012.

Gu-Yeon Wei Gu-Yeon Wei is Gordon McKay Professor of Electrical Engineering and Computer Science in the School of Engineering and Applied Sciences (SEAS) at Harvard University. He received his BS, MS, and PhD degrees in Electrical Engineering from Stanford University in 1994, 1997, and 2001, respectively. His research interests span multiple layers of a computing system: mixed-signal integrated circuits, power electronics, computer architecture, and compilers for automatic code parallelization. Research efforts primarily focus on opportunities across these layers to develop energy-efficient solutions for a broad range of systems from flapping-wing microrobots to large-scale servers.