A 7.5-GS/s 3.8-ENOB 52-mW flash ADC with clock duty cycle control in 65nm CMOS

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Abstract

A 7.5-GS/s 4.5-bit analog-to-digital converter (ADC) in 65nm CMOS is presented. A two-stage track-and-hold (TAH) with clock duty cycle control reduces bandwidth requirements on the slow TAH output to enable high sampling rates with low power consumption. The 7.5-GS/s flash ADC consumes 52-mW and occupies 0.01-mm^2. Clock duty cycle control improves ENOB from 3.5 to 3.8 with an input sinusoid at the Nyquist frequency.

Keywords: ADC, high sampling rate, low power, clock duty cycle control, two-stage track and hold

Introduction

As demand for data rates increases, receiver front-ends that rely on high-speed (multi-GS/s), low-resolution (4-5 bit) ADCs are being considered for high-speed backplane communication to fully exploit the benefits of sophisticated digital signal processing techniques [1]. However, large area and high power consumption of fast ADCs are major concerns. This work describes a 6-7.5 GS/s, 4.5-bit flash ADC with low power consumption of 48-52 mW, which can be interleaved for 12-15 Gbps serial communication, or used directly at 6-7.5 Gbps.

Architecture and Implementation

Fig. 1 presents the proposed 4.5-bit flash ADC architecture. Designing a fast track and hold (TAH) for high-speed flash ADCs is challenging due to large capacitive loading on the TAH output as a result of the 22 parallel comparators. To overcome bandwidth limitations, the proposed ADC relies on a 2-stage TAH structure [2]. Fast tracking is possible in the first stage since it is lightly loaded by the second stage that buffers it from the large capacitive loading of the comparators.

Fig. 2(a) illustrates the proposed 2-stage TAH circuit schematic implemented in CMOS. Each TAH stage consists of PMOS switches, including dummy switches to cancel charge injection, and a CML buffer. The switches in the two stages are driven by complementary clocks (*clk* and *clk_b*). The cross-coupled capacitors, added across the CML buffers, help reduce glitching on the outputs due to C_{gd}.

Fig. 2(b) presents signal timing diagrams of annotated nodes in the schematic and clock waveforms that illustrate the proposed clock duty cycle control. Since the second stage tracks a settled voltage held by the first stage, this topology accommodates the slower, heavily-loaded second stage. In order to aggressively push sampling frequencies (to 7 GS/s and higher) the proposed design investigates clock duty cycle control to effectively extend tracking time of the second stage by widening the duty cycle of TAH clock. A duty cycle controller, with 2-bit thermometer coding (00, 01, and 11) provides 50-58% duty cycle range (in simulation). Widening duty cycle from 50% to 58% reduces the second stage's bandwidth requirement by 14%, which, in other words, translates to a 14% increase in sampling rate and power savings. Simulations of the extracted layout show the TAH and duty cycle control block each consume a small fraction (8%) of the total ADC power.

This relatively simple modification significantly improves tracking performance at high sampling rates, obviates extra loading on the first stage, and avoids large power and area penalties. However, it is important to guarantee sufficient hold time for comparators (clocked on the rising edge of *clk_b*) to properly resolve.

To further improve speed and reduce power, each comparator cell uses minimum-size input devices to minimize total capacitive loading on the output of the second TAH stage. To compensate for resulting nonlinearities and offsets in the comparator and TAH buffer due to device mismatch, the ADC design employs two compensation techniques—reference pre-distortion (by adjusting the resistor ladder) [3] and comparator reassignment [4]—both calibrated during startup. Measurements made before and after DC calibration show INL improves from 2.6 to 0.38 LSB and DNL improves from 3.4 to 0.35 LSB, as listed in Table I.

Measurements

The ADC was fabricated in a 65nm bulk CMOS process and tested at wafer level (Fig. 5). For all measurements, 3 out of 22 comparator outputs were selected at a time through three 8:1 multiplexers (due to pad limitations) and captured off-chip using a real-time oscilloscope. The sine wave input, sampling clock, and oscilloscope trigger sources were synchronized with a clean reference source. The final ADC output was reconstructed by aligning the 22 comparator outputs, which were measured at different times, and analyzed in MATLAB.

Fig. 3(a) plots the measured SNDR at 6 GS/s across a range of input sinusoid frequencies. Fig. 3(b) plots the measured SNDR at different sampling rates with and without clock duty cycle control. For each sampling rate, measurements used a worst-case input frequency for the second TAH stage—at the Nyquist frequency with small offset. Fig. 3(b) shows that clock duty cycle control improves SNDR performance, which remains above 24 dB up to 7.5 GS/s. Fig. 3(c) presents the FFT output at 7.5 GS/s with a 3.835-GHz sine wave input and duty cycle control (code=01). An SNDR of 24.5 dB translates to an ENOB of 3.8. The ADC consumes 52 mW at 1.1-V, resulting in a figure of merit (FOM) of 0.497 pJ/conversion.

Fig. 4 compares this work with previously reported ADCs found in [5]. The FOM of this work is at least 4 times better than ADCs with comparable sampling rates. While this work focuses on a single ADC path, the 2-stage TAH topology facilitates interleaving with low power penalty because of the small capacitive loading imposed by the first TAH stage. When interleaved, much higher sampling rates with small increase in FOM are possible.

Table I summarizes the measured ADC performance. The 2-stage TAH design, with clock duty cycle control, and small comparator devices, with calibration, lead to a low-power Nyquist rate ADC for high-speed serial communication.

References

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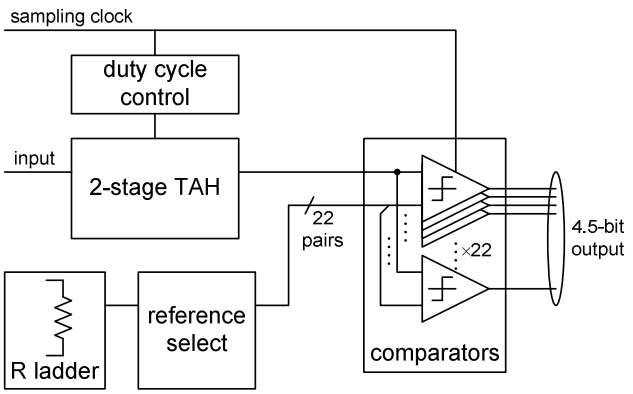

Fig. 1 Block diagram of the 4.5-bit flash ADC.

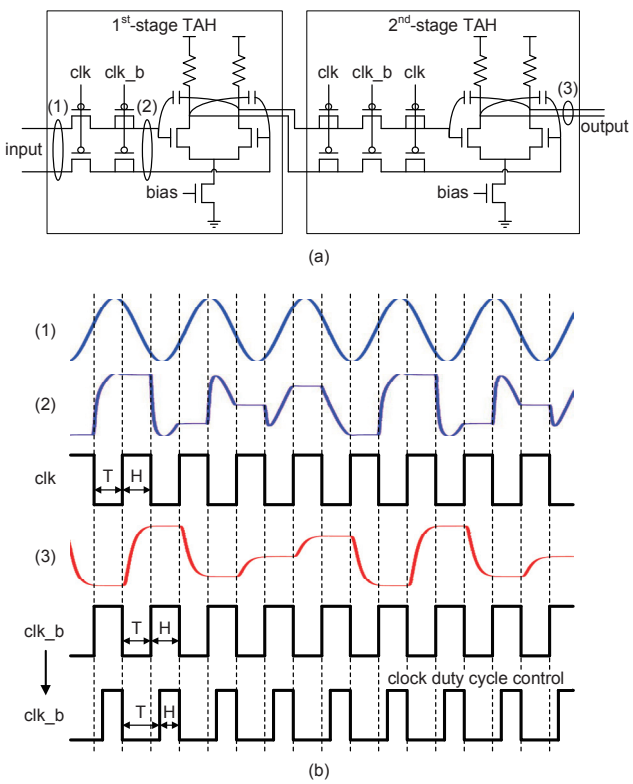

Fig. 2 Two-stage TAH with clock duty cycle control: (a) 2-stage TAH circuit, (b) 2-stage TAH timing diagram and duty cycle control.

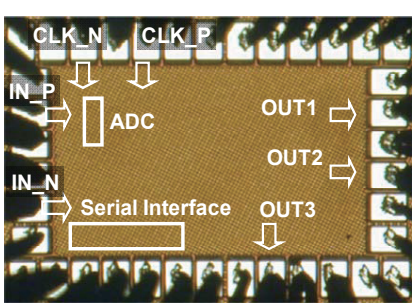

Fig. 5 Die photo (pad pitch: 100 µm).

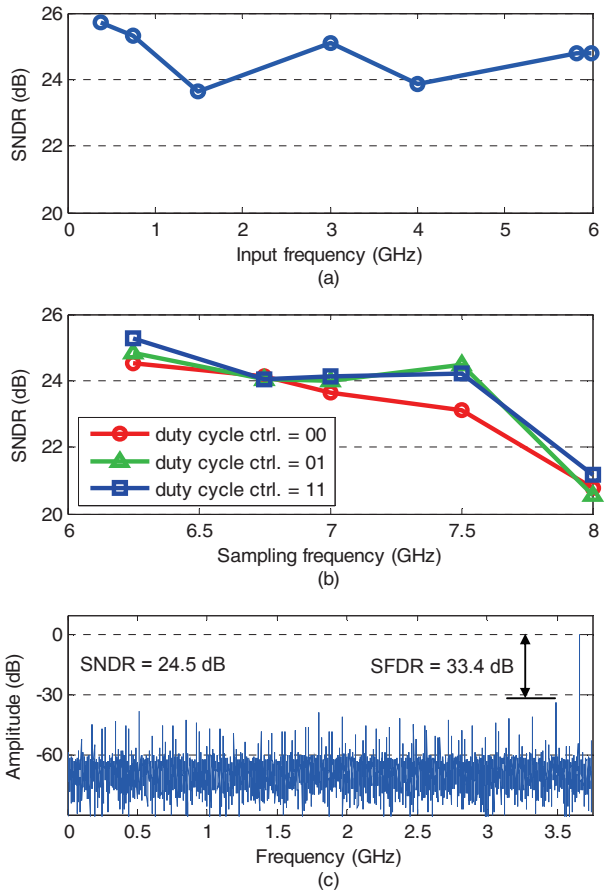

Fig. 3 Measured ADC performance: (a) SNDR at 6 GS/s vs. input frequency, (b) SNDR vs. sampling frequency (with 2-bit thermometer duty cycle control), and (c) FFT plot at 7.5 GS/s. Both (b) and (c) were measured with input sinusoid at Nyquist frequency.

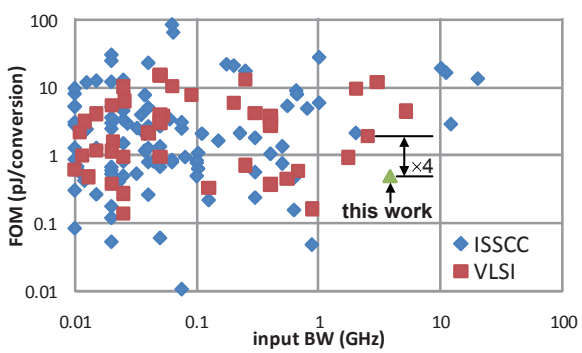

Fig. 4 FOM vs. input bandwidth: comparison to prior work in [5].

Table I Performance Summary

Technology	65 nm CMOS	
Supply	1.1 V	
ADC Active Area	65 µm x 162 µm = 0.01 mm^2	
INL (before/after calibration)	2.6 LSB/0.38 LSB	
DNL (before/after calibration)	3.4 LSB/0.35 LSB	
Input Range	0.8 V_{pp} (differential)	
Sampling Rate	7.5 GS/s	6.25 GS/s
Power	52 mW	47.5 mW
ENOB (w/ duty cycle ctrl.)	3.8	3.9
ENOB (w/o duty cycle ctrl.)	3.5	3.8
FOM	0.497 pJ/conv.	0.508 pJ/conv.