## 21.5 A 3-to-5V Input 100V$_{pp}$ Output 57.7mW 0.42% THD+N Highly Integrated Piezoelectric Actuator Driver

Simon Chaput, David Brooks, Gu-Yeon Wei

Harvard University, Cambridge, MA

Piezoelectric actuators are used in a growing range of applications, e.g., haptic feedback systems, cooling fans, and microrobots. However, to fully realize their potential, these actuators require drivers able to efficiently generate high-voltage (>100V$_{pp}$) low frequency (<300Hz) analog waveforms from a low-voltage source (3-to-5V) with small form factor. Certain applications, such as piezoelectric (PZT) cooling fans, further demand low distortion waveforms (THD+N < 1%) to minimize sound emission from the actuator. Existing solutions for small PZT drivers typically rely on designs comprising a power converter to step up a low voltage followed by a high-voltage amplifier [1,2,3]. Although envelope tracking can help reduce amplifier power [3], none of these designs can recover the energy stored on the actuator to maximize efficiency. And while a differential bidirectional flyback converter [4] can recover energy, it requires four inductors, thereby incurring large size penalty. This paper introduces a single-inductor, highly integrated, bidirectional, high-voltage actuator driver that achieves 12.6× lower power and 2.1× lower THD+N at a similar size to the currently available state-of-the art solution [1]. Measured results from an IC prototype demonstrate 200Hz sinusoidal waveforms up to 100V$_{pp}$ with 0.42% THD+N from a 3.6V source while dissipating 57.7mW to drive a 150nF capacitor. Beyond PZT actuators, the IC can also drive any type of capacitive load, e.g., electrostatic and electroactive polymer actuators.

Figure 21.5.1 presents the proposed driver comprising the driver IC, one external inductor (L), one filter capacitor ($C_{FILTER}$), and a sense resistor ($R_{SENSE}$). The driver IC further comprises three main blocks: A first bidirectional synchronous power converter stage generates a folded waveform ($V_{FOLDED}$) from a low-voltage source ($V_{IN}$) by transferring small increments of energy to (in forward-boost mode) and from (in reverse-buck mode) the load, similar to [5]. A second (full-bridge) stage unfolds the waveform via four high-voltage switches ($M_{3\text{-}6}$) to generate a full-swing (-50V to 50V) signal across the load. Lastly, an embedded controller implements several techniques to achieve low power and low distortion.

The driver topology balances power, size, and performance to enable the use of high voltage actuators with minimal overhead. Referencing the full-bridge stage to $V_{IN}$ enables low-distortion zero crossings with a two-switch power converter topology to generate voltages above GND. By avoiding four-switch buck-boost or two-switch inverting buck-boost topologies, the IC has smaller die area (i.e., two switches) or simpler die biasing (i.e., no negative supply), respectively. Although direct current sensing through an external $R_{sense}$ dissipates more power, it enables accurate bidirectional inductor current monitoring across all operating conditions.

The controller implements multiple techniques to reduce DC loss ($P_{DC}$), switching loss ($P_{SW}$), and improve waveform quality. First, boundary conduction mode (BCM) operation reduces losses and minimizes the size of L. Moreover, L is sized to minimize switching frequency ($f_{sw}$) while achieving a target THD+N and signal bandwidth. A smaller L will increase $f_{sw}$ thus increasing $P_{sw}$, but it will enable the controller to track the reference waveform more accurately, thus reducing the THD+N. A higher $f_{sw}$ will also enable more energy to be transferred to/from the load, thus increasing output signal bandwidth. Second, $P_{SW}$ is further reduced by zero voltage switching (ZVS) of 60V high-voltage devices $M_1$ and $M_2$. In boost mode, ZVS is possible with conventional synchronous switching. However, in reverse-buck mode, the controller implements pseudo-resonant synchronous (PRS) operation to guarantee ZVS of $M_2$. Transistor $M_1$ stays ON until the inductor current ($I_L$) reaches a current threshold (at $t_3$) required to charge the switching node to $V_{FOLDED}$ ($t_3$-$t_4$). Hence, $M_2$ turns ON with ZVS and no discontinuity appears in the current waveform. The controller sets the current threshold on a cycle-by-cycle basis to accurately generate the folded waveform while reducing switching losses. The digital controller implements an adaptive PI algorithm that dynamically adjusts its gains with respect to state variables such as output voltage and switching frequency of the driver, thus, enabling more accurate tracking of the reference waveform over the full range of output voltage.

Figure 21.5.2 presents the full-bridge stage and its drivers. Since 60V high-voltage transistors $M_{3\text{-}6}$ switch at a low rate (100s of Hz) to construct the final waveform ($V_{OUT}$), the two half-bridge drivers can be small, incurring minimal area penalty. To avoid the complexities of conventional high-side drivers, the driver IC uses a compact charge pump ($C_1$, $D_1$, and $D_2$) to drive and maintain $V_{GS,\,M3}$ at ≈4V when $M_3$ is ON. This design can generate arbitrary low-frequency waveforms (down to DC) with 100V$_{pp}$ amplitude.

Figure 21.5.3 plots a 200Hz, 99.2Vpp sinusoid measured across a 150nF capacitor load driven by the test chip while consuming 57.7mW from a 3.6V source. The prototype achieves a THD+N of 0.421% within a 1MHz bandwidth without the need for an output filter (unlike class-D amplifiers [2]). The spectrum shows an attenuation of 53.5dB between the fundamental frequency and the second harmonic. The spectrum also shows the converter's switching noise–in the hundreds of kHz range–does not impact signal quality.

Figure 21.5.4 compares the measured $V_{IN}$ supply current required to drive a 150nF capacitor versus a PZT actuator at 200Hz across a range of input and output voltage conditions. The lower effective capacitance of the PZT actuator results in lower supply current, but both sets of current measurements scale quadratic with output swing. The bottom row plots the measured THD+N across the same conditions. While the THD+N hovers around 0.5% for signals greater than 50Vpp, distortion increases for lower output amplitudes because the controller was optimized for high amplitude waveforms. In addition to low-distortion sinusoids, the prototype driver can also generate arbitrary and complex waveforms, illustrated by Fig. 21.5.5, which broadens the range of possible applications (e.g., haptic). However, discontinuous waveforms (e.g., square waves) are slew-rate limited due to the high instantaneous power required at the edges.

Figure 21.5.6 presents a comparison between a state-of-the-art driver [1] and the proposed driver for three different loads. An ideal capacitor is the best-case load for our chip, because it does not transform energy to motion (i.e., more energy can be recovered) and does not exhibit resonant behavior. Therefore, we also compare results for a PZT-based fan and a haptic PZT actuator in order to compare real world performance. For [1], its demo board [6] was used to experimentally measure the power required to drive these two PZT actuators (minus the power consumed by demo board support circuitry). The test chip achieves 12.58× (capacitor), 6.44× (fan), and 10.83× (haptic) power reduction compared to [1] while consistently achieving lower THD+N. The power improvement is lower for the fan, because the PZT actuator operates at resonance and, therefore, dissipates more energy. Figure 21.5.7 shows the micrograph of the chip fabricated in a 0.18µm high-voltage SOI CMOS technology.

Low power, small size, and good signal fidelity have significant impact at the system level. Multi-actuator haptic feedback systems for wearables struggle to handle the power budget and heat dissipation from available actuator drivers. In the case of a piezo fan, low power consumption is essential for the use of the fan in portable electronics. Good signal fidelity is critical for piezo fans in order to achieve low acoustic noise operation; a requirement in most applications. Signal bandwidth up to 300Hz is sufficient in those applications. It avoids generating noise (fan) and corresponds to the bandwidth where the human is the most sensitive to vibrations (haptic). Higher signal bandwidth, slew rate, and output voltage range can be achieved by scaling the design.

*Acknowledgements:*
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*References:*
[1] Texas Instruments, DRV8662, "Piezo haptic driver with integrated boost converter," Datasheet, Dec. 2014. Available at: <www.ti.com>.
[2] Fairchild Semiconductor, FAN8831, "Sinusoidal piezoelectric actuator driver with step-up DC-DC converter," Datasheet, Dec. 2014.
Available at: <www.fairchildsemi.com>.
[3] M. Lok, et al., "A power electronics unit to drive piezoelectric actuators for flying microrobots", *IEEE CICC*, pp. 1-4, 2015.
[4] R. Ramabhadran, et al., "A low power consumption driver with low acoustics for piezoelectric synthetic jets," *IEEE ECCE*, pp. 2692-2697, 2013.
[5] A.M. Salamah, et al., "Single-phase voltage source inverter with a bidirectional buck-boost stage for harmonic injection and distributed generation," *IEEE Trans. Power Electronics,* vol. 24, no. 2, pp. 376-387, Feb. 2009.
[6] Texas Instruments, DRV8662, "Piezo haptics driver evaluation module", User's Guide, Mar. 2016. Available at: <www.ti.com>.

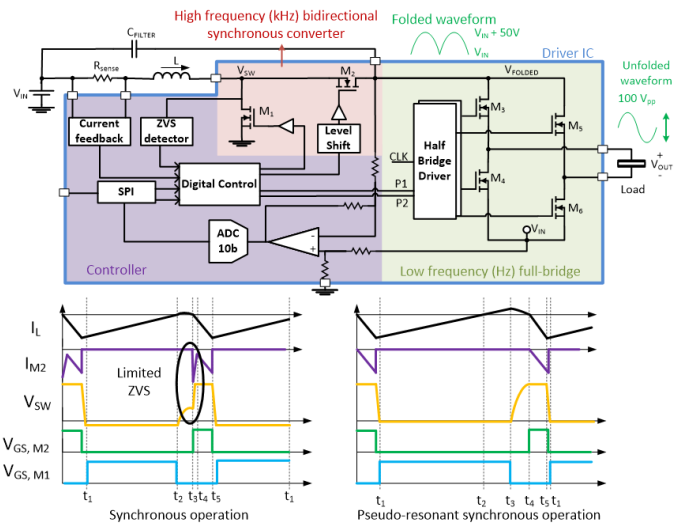


**Figure 21.5.1: Bidirectional synchronous buck-boost driver architecture (top). The waveforms illustrate the need for PRS operation to achieve ZVS (bottom).**

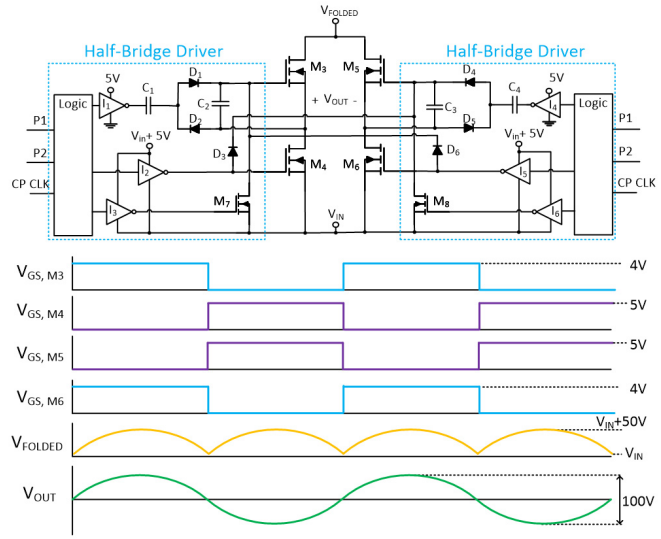


**Figure 21.5.2: Control circuit for the full-bridge power stage.**

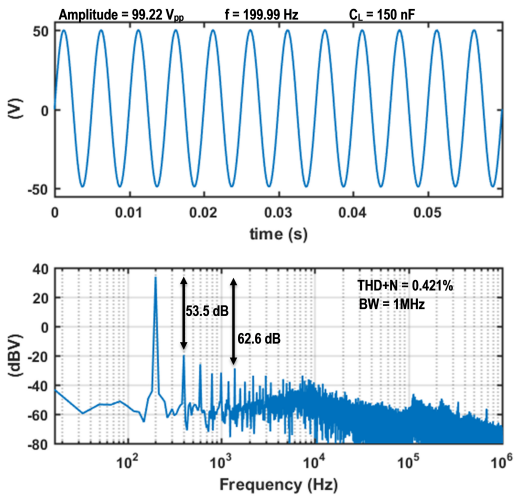


**Figure 21.5.3: Time domain waveform and corresponding spectrum of a 200Hz 99.2$V_{pp}$ sine generated across a 150nF load capacitor from a 3.6V input voltage.**

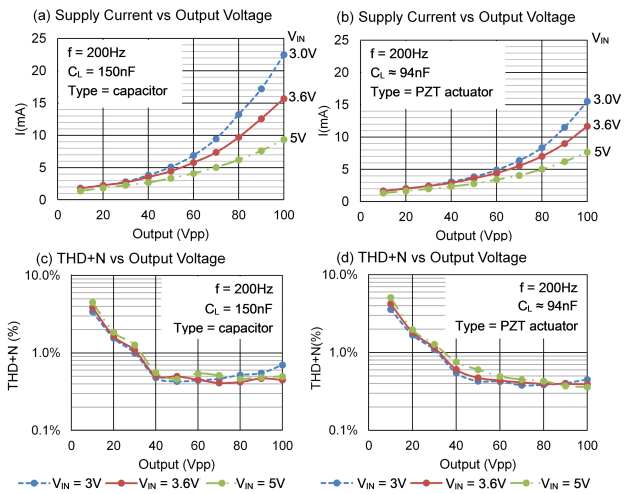


**Figure 21.5.4: Measured input current and THD+N within a 1MHz bandwidth for a capacitor (a,c) and a PZT actuator (b,d).**

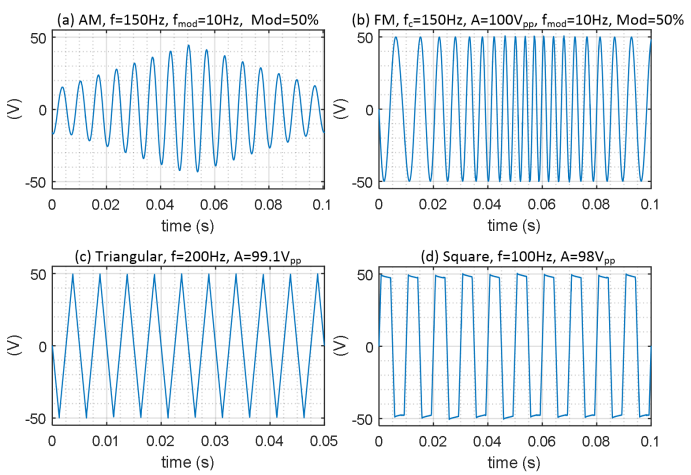


**Figure 21.5.5: Measured waveforms ($V_{IN}$ = 3.6V, $C_L$ = 150nF). Overshoot in discontinuous waveforms (c, d) limits the output amplitude to avoid triggering overvoltage detection logic.**

| | [1]* | This Work | [1] | This Work | [1] | This Work |
|---|---|---|---|---|---|---|
| Technology | - | 0.18µm | - | 0.18µm | - | 0.18µm |
| Load type | Capacitor | | Piezoelectric fan | | Haptic Actuator | |
| Load Part Number | N/A | | GE DCJ unit 3044 | | Midé PPA-2014 | |
| Capacitive load (nF) | 330 | | ≈170 | | ≈94 | |
| Package | QFN 4x4 mm | | QFN 4x4 mm | | QFN 4x4 mm | |
| Inductor | LPS4018 | | LPS4018 | | LPS4018 | |
| Inductor value (µH) | 4.7 | 100 | 4.7 | 100 | 4.7 | 100 |
| $C_{FILTER}$ (nF) | 100 | 10 | 100 | 10 | 100 | 10 |
| Input Voltage (V) | 3.6 | | 5 | | 3.6 | |
| Frequency (Hz) | 150 | | 150 | | 150 | |
| Output Voltage (Vpp) | 100 | | 100 | | 100 | |
| Resonant Frequency | N/A | | Yes | | No | |
| Power (mW) | 1080 | 85.8 | 640.7 | 99.5 | 351.6 | 32.47 |
| THD+N (%) | 1.2 | 0.56 | 1.15 | 0.36 | 1.12 | 0.33 |

**Figure 21.5.6: Performance summary and comparison. Data for [1]* with a capacitor load extracted from the datasheet. All other data is measured.**

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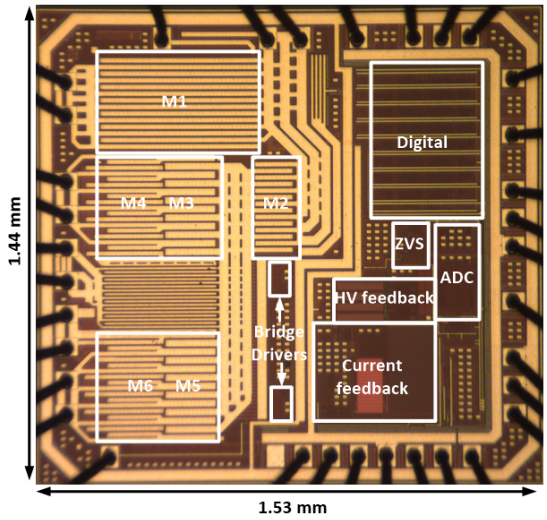


**Figure 21.5.7: Micrograph of the test chip fabricated in a 0.18µm high-voltage SOI CMOS process.**


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