A $20\mu W$ 10MHz Relaxation Oscillator with Adaptive Bias and Fast Self-Calibration in 40nm CMOS for Micro-Aerial Robotics Application

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***Abstract*—Efficient actuation control of flapping-wing microrobots requires a low-power frequency reference with good absolute accuracy. To meet this requirement, we designed a fully-integrated 10MHz relaxation oscillator in a 40nm CMOS process. By adaptively biasing the continuous-time comparator, we are able to achieve a power consumption of $20\mu W$, a 68% reduction to the conventional fixed bias design. A built-in self-calibration controller enables fast post-fabrication calibration of the clock frequency. Measurements show a frequency drift of 1.2% as the battery voltage changes from 3V to 4.1V.**

I. Introduction

Flapping-wing aerial microrobots using piezoelectric actuators have been demonstrated experimentally and have shown great potential towards autonomous flight [4]. The importance of energy and weight tradeoffs in these applications demand an efficient actuation scheme. To the first order, the aerial robot can be modeled as a linear system with many vibration modes, the lowest of which corresponds to the wing flapping motion. Driving the actuator at the resonant frequency of this vibration mode maximizes both the wing stroke and the lift force [3]. Since the actuator drive signals are generated by direct digital synthesis from a fixed-frequency reference clock, their frequency accuracy critically depends on the timing accuracy of this clock source. Moreover, the pulse control signals for the inductor-based power electronics that amplify the actuator drive signals are also derived from the same clock reference. Their pulse width is chosen to maximize the efficiency of the power electronics and, thus, is also sensitive to clock timing error. For these two reasons, the reference clock needs to maintain good frequency accuracy throughout the operation of the microrobots. Nevertheless, autonomous microrobots are solely powered by a compact Li-Polymer battery whose output voltage is not constant due to discharge, therefore the reference clock must also provide a stable frequency across variations of the battery voltage.

This paper presents a 10MHz relaxation oscillator, implemented in a standard 40nm CMOS process, as the on-chip clock source for the power actuators in microrobotic applications. The relaxation oscillator (RO) consumes $20\mu W$ of power and occupies $0.017mm^2$ of silicon area, meeting the stringent power and weight budget of the robotic system. We implemented a novel technique of adaptively adjusting the bias current of the comparator to reduce comparator power by 68%. A built-in self-calibration controller speeds up post-fabrication test, which exploits the linear relationship between the clock period and the digital control code to minimize calibration time. Measurements show that the output frequency of our RO varies less than 1.2% as the battery discharges from 4.1V to 3V.

The oscillator architecture and the underlying circuits are presented in Section II, followed by the measurement results in Section III. Section IV summarizes the oscillator performance.

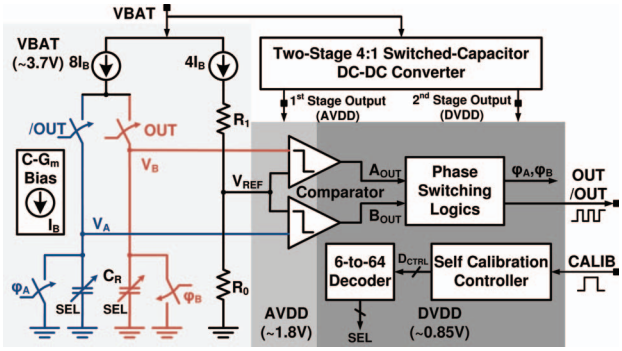

Fig. 1: System architecture of the on-chip relaxation oscillator

II. Oscillator Architecture

Fig. 1 shows the top-level system architecture of the relaxation oscillator designed for the power actuators in microrobotic applications. It consists of circuit blocks in three different voltage domains as indicated by the distinctively shaded area in the diagram. Since the oscillator is integrated with a larger System-on-Chip (SoC) that functions as the 'brain' of the microrobot [8], it interfaces with the voltage levels generated by a 4:1 switched-capacitor (SC) DC-DC converter in the 'brain' SoC. With two cascaded 2:1 SC stages, the DC-DC converter converts the battery voltage (VBAT) around 3.7V to lower I/O voltage (AVDD) at 1.8V and digital voltage (DVDD) at 0.85V [7].

In the VBAT domain, a constant-G_m bias circuit (Fig. 2) generates the bias current (I_B), which is mirrored to alternatively charge the two-grounded capacitors, as well as to generate the reference voltage (V_{REF}). Both the constant-G_m bias circuit and the current mirror include multiple cascoded transistors to take advantage of the abundant headroom at the higher battery voltage for improved mirror accuracy.

Fig. 3 illustrates the basic operation of the relaxation oscillator. The two-grounded capacitors are periodically linearly charged by I_B and discharged to ground. The voltages across them, V_A and V_B, are compared to $V_{REF} = I_B R_0$, and the output of the comparators are latched and fed to phase switching logic blocks. These blocks generates the clock outputs, OUT and /OUT, along with the switching signals $\varphi_A = OUT \ \& \ DLY$ and $\varphi_B = \overline{OUT \mid DLY}$, where DLY is OUT delayed by a small time τ. The delayed discharge ensures minimal disturbance of V_A and V_B when they cross V_{REF}. The continuous-time comparators are powered by AVDD, but their outputs are level-shifted to the DVDD domain. The bias V_{EN} and I_D are explained in Section II-A.

In addition to the phase switching logic, also residing in the DVDD domain are the self calibration controller and a 6-to-64 decoder that converts a 6-bit binary control code D_{CTRL} to a 64-bit thermometer code SEL to select the array of capacitors ($C_R = C_{OFFSET} + D_{CTRL}C_0$).

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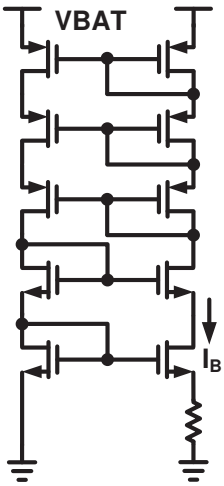

Fig. 2: C-G_m bias circuit

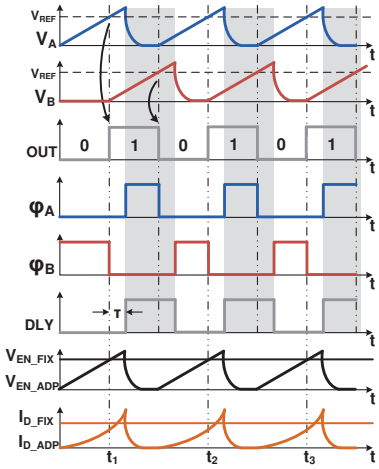

Fig. 3: Timing graph of the waveforms in the relaxation oscillator

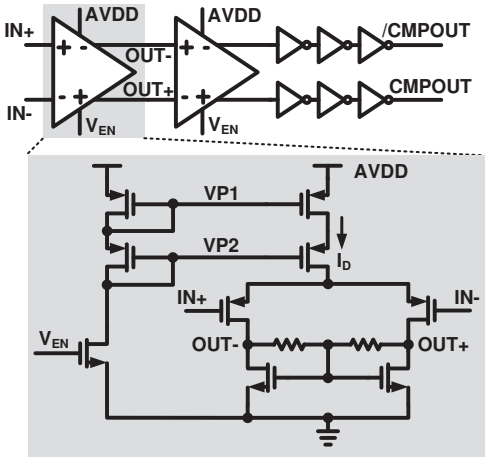

Fig. 4: Schematic of the continuous-time comparator

According to Fig. 3, the oscillation period T_{CLK} is determined by the time it takes V_A and V_B to charge to V_{REF} plus the comparator and buffer delay (τ_{CP}), hence:

$$T_{CLK} = 2(\frac{V_{REF}C_R}{MI_B} + \tau_{CP}) = R_0C_R + 2\tau_{CP} \qquad (1)$$

where M is the current mirror ratio between the branch current that charges up the grounded capacitors and the branch current that generates V_{REF}. In our design, $M = 2$, $R_0 = 400K\Omega$, $C_0 = 3.5fF$, $C_{OFFSET} = 32C_0$, and $\tau_{CP} \approx 2.5ns$, all of which are subject to process variation.

A. Adaptively-Biasing of the Comparator

As shown in Fig. 4, the continuous-time comparator used in the oscillator consists of two cascaded differential amplifiers with output inverter buffers. The differential amplifiers are supplied by the 1.8V AVDD, and a bias voltage V_{EN} determines the bias current I_D for the amplifier. The PMOS input differential pair is chosen because the input signals to the comparator (V_A, V_B, $V_{REF} = 0.6V$) fall in the range of 0V and 0.7V. The resistive common-mode feedback is applied to control the DC level at the output so that it is level-shifted to interface with the inverter buffers in the 0.85V DVDD domain.

The continuous-time comparators consume a significant portion of the total system power. According to (1), the comparator delay affects the oscillation period and should be minimized to reduce the associated non-idealities, such as supply sensitivity and nonlinearity of the clock period versus the control code. In the conventional design where V_{EN} is fixed, this is achieved by increasing the bias current I_D to improve the gain-bandwidth-product (GBP) of the differential amplifier, which leads to higher power consumption.

However, a fixed bias configuration can be highly inefficient for comparators used in relaxation oscillators, because the only performance-critical comparison happens as V_A (or V_B) crosses V_{REF}, and power is largely wasted when the voltage across the capacitor is far away from the reference voltage. Instead, the adaptive bias configuration we implemented takes advantage of the saw tooth shape waveform of the voltages across C_R (i.e. V_A and V_B) and uses them as the bias voltage V_{EN} for the differential amplifiers in their respective comparators. This is illustrated in Fig. 3. The adaptive biasing technique ensures good comparator performance during the critical comparison periods of operation (e.g. t_1, t_2, t_3 for V_A comparator), and saves power by significantly reducing I_D during the rest of the operation.

B. Fast Built-in Self-Calibration

The clock period of the relaxation oscillator depends on R_0, C_R, and τ_{CP}, making it susceptible to process variation in deep sub-micron technology node. To achieve better frequency accuracy, post-fabrication calibration is used by counting the number of the oscillation cycles during a fixed timing window (T_{CAL}) from an external calibration signal (CALIB in Fig. 1) and then adjusting the digital control code (D_{CTRL}) accordingly. Since test time is an important cost metric, a fast and scalable calibration scheme is desirable for low cost integrated oscillators. Existing calibration schemes employ binary search that successively refines D_{CTRL} one bit per step from MSB to LSB to speed up the calibration, as compared to a linear search. In this way, the time needed for calibration grows linearly with the number of bit in D_{CTRL}. The downside of a binary search is its vulnerability to one-time counting error, as D_{CTRL} is resolved one bit at a time.

It is possible to achieve faster calibration than the binary search by exploiting the linear relationship between D_{CTRL} and T_{CLK} in the relaxation oscillator:

$$\begin{aligned} T_{CLK} &= R_0(C_0D_{CTRL} + C_{OFFSET}) + 2\tau_{CP} \\ &= R_0C_0(D_{CTRL} + D_{OFFSET}) \end{aligned} \qquad (2)$$

where $D_{OFFSET} = \frac{C_{OFFSET}}{C_0} + \frac{2\tau_{CP}}{R_0C_0}$, and R_0, C_0, and D_{OFFSET} are all subject to variation. Assume T_{CAL} is chosen such that N^* cycles will be counted after the digital control code reaches its final calibrated value D^*_{CTRL}:

$$T_{CAL} = N^*T^*_{CLK} = N^*R_0C_0(D^*_{CTRL} + D_{OFFSET}) \qquad (3)$$

If we initialize the digital control code to a predetermined value D^0_{CTRL} and count the cycles during T_{CAL} to be N^0, we get:

$$T_{CAL} = N^0R_0C_0(D^0_{CTRL} + D_{OFFSET}) \qquad (4)$$

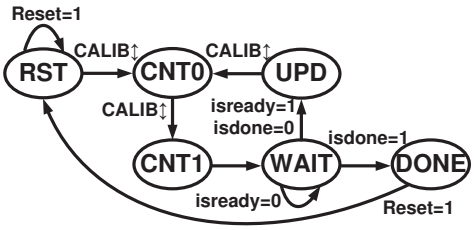

Fig. 5: State transition graph of the self-calibration controller

Equating the right hand side of both (3) and (4), we are able to derive D^*_{CTRL} in an analytical expression:

$$D^*_{CTRL} = \frac{N^0(D^0_{CTRL} + D_{OFFSET})}{N^*} - D_{OFFSET} \quad (5)$$

The real value of D_{OFFSET} is unknown due to process variation, but in design time, we can estimate its statistical average, D^0_{OFFSET}, from Monte-Carlo simulation, which can then be used to iteratively approximate the equation in (5):

$$D^{n+1}_{CTRL} = \frac{N^n(D^n_{CTRL} + D^0_{OFFSET})}{N^*} - D^0_{OFFSET} \quad (6)$$

where D^n_{CTRL} and N^n are the digital control code and the number of counts during the n^{th} step of the calibration. The ASIC implementation of the update equation (6) is simple, because N^* can be chosen to be a power of 2, so that division is reduced to right-shift operations. For example, in our design, $N^* = 128$. Formal mathematical derivation proofs that (6) always converges geometrically to D^*_{CTRL} in fewer than 3 steps regardless of the number of bit in D_{CTRL}.

Based on the update equation above, we implemented the self-calibration controller for the oscillator as a state machine that counts the number of clock cycles during T_{CLK} at each calibration step and updates D_{CTRL} accordingly. Fig. 5 illustrates the state transitions in the controller. The system is first initialized in the reset state (RST), waiting for the external CALIB signal transition (CALIB↕) to enter into the counting states (CNT0 and CNT1). The reason they are separated into CNT0 and CNT1 is because we expect CALIB to be square waves with a period of T_{CAL} in our testing setup, instead of burst pulse with a width of T_{CAL}. If the system is ready (isready=1), the controller enters the update state (UPD) to calculate the digital control code (D_{CTRL}) for the next calibration step. When the number of counts during the counting states reaches N^*, the calibration is done (DONE).

III. Experimental Results

The relaxation oscillator was fabricated in TSMC's 40nm standard digital process as part of a prototype SoC chip for aerial microrobots. As shown in the zoom-in layout of the chip in Fig. 6, two versions of the oscillator have been taped out–one with the proposed adaptive biasing of the comparators and the other with conventional fixed biasing. In this way, a fair comparison of power and performance can be made.

The aggregated power consumption from all three voltage domains has been measured for both the fixed and adaptive bias designs while sweeping the battery voltage from 3V to 4.1V, and the results are plotted in Fig. 7. At the nominal $VBAT = 3.7V$, our oscillator consumes less than $20\mu W$, as compared to a conventional fixed bias design that consumes

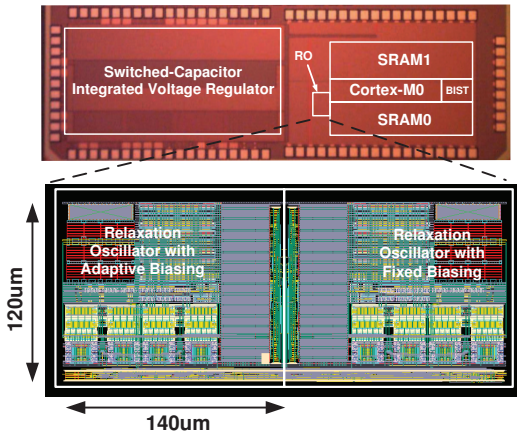

Fig. 6: Die photo and layout of the relaxation oscillator

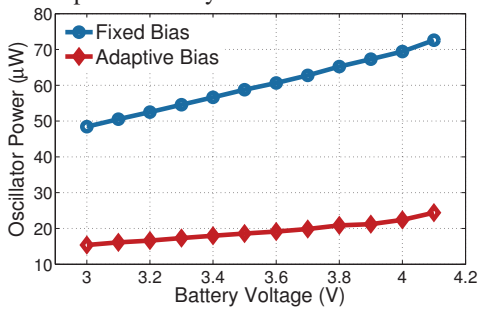

Fig. 7: Oscillator power with fixed and adaptive bias

more than $62.8\mu W$. A 68% power reduction is achieved across the entire battery voltage range.

To show that the power savings do not penalize oscillator performance, we first measured the supply sensitivity of the oscillator at different digital control codes. In Fig. 8, our oscillator with adaptive bias shows a typical frequency variation of 1.2%, outperforming the fixed bias oscillator with 2.0% variation over the battery voltage from 3V to 4.1V.

Finally, the period jitter for both oscillator designs was measured at 10MHz. The jitter histogram scope capture in

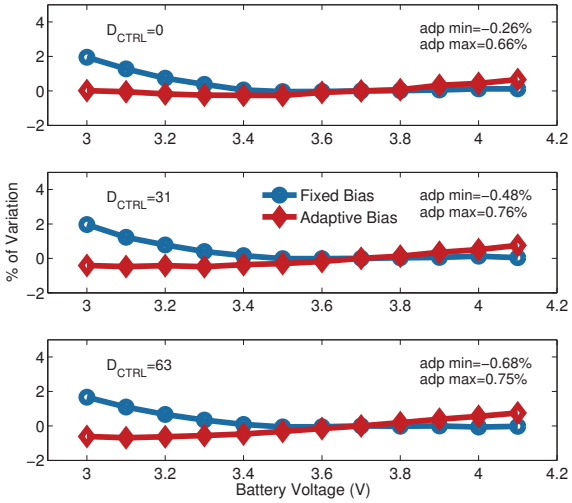

Fig. 8: Percentage variation of the oscillation frequency over changing battery voltage

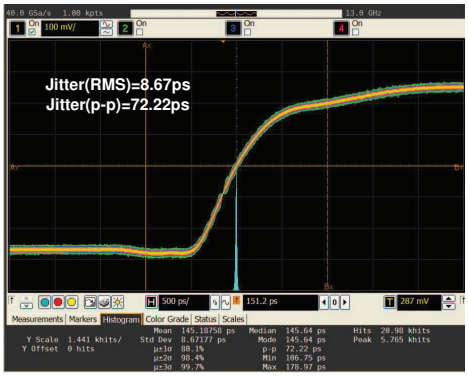

Fig. 9: Measured jitter for the oscillator with adaptive bias

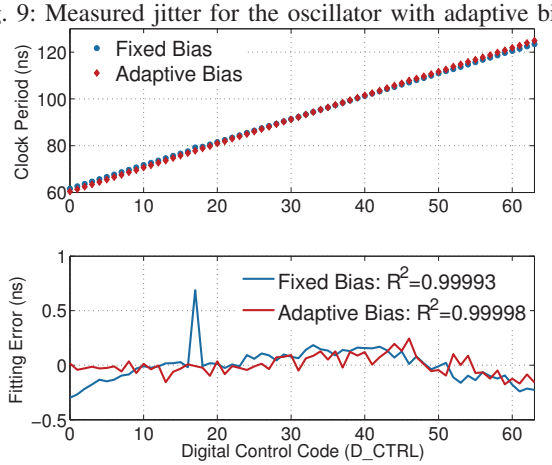

Fig. 10: Oscillation period changes linearly with D_{CTRL}

Fig. 9 shows a random RMS jitter of 8.67ps and a peak-to-peak jitter of 72.22ps for our oscillator with adaptive bias. The fixed bias design yields a similar jitter performance of 8.67ps RMS jitter and 77.78ps of peak-to-peak jitter.

Fig. 10 confirms the linear relationship between the clock period and the digital control code with negligible fitting error, making the proposed faster calibration scheme possible.

In addition to the calibration scheme based on (6), a binary mode was also implemented in the self-calibration controller to allow fair comparison. Fig. 11 shows how the digital control code (D_{CTRL}) converges to its final calibrated value at each step, when the CALIB signal width is set at $T_{CAL} = 10.31\mu s$, along with the corresponding oscillation period (left axis) and the number of cycle counts during T_{CAL} (right axis). Compared to the binary search algorithm, the proposed calibration scheme converges within 3 steps and are more robust to counting errors. The top plot in Fig. 11 also captures the vulnerability of the binary search algorithm to random noise: in step 5, a counting error is made that leads D_{CTRL} to resolve incorrectly to 15 instead of 13.

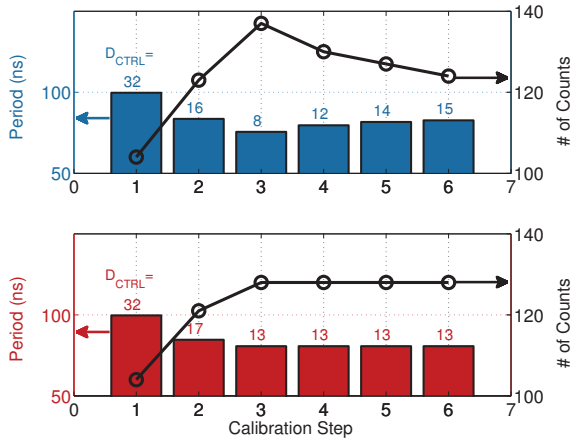

Fig. 11: Convergence of D_{CTRL} with each calibration step

Table I compares performance of the proposed relaxation oscillators to prior work. With the lowest power consumption, our design delivers superior jitter performance and comparable supply insensitivity. We are also the only design in the table to have built-in self calibration.

IV. Conclusion

A low-power relaxation oscillator with adaptive bias and fast self-calibration was implemented in 40nm CMOS. With $20\mu W$ power consumption, it achieves 68% power reduction over the conventional fixed-bias design. Clock period fluctuations due to changes in battery supply voltage is within 1.2% over 3V to 4.1V, and the periodic RMS jitter is 8.7ps. The proposed algorithm implemented in the built-in calibration controller allows geometrically fast automatic oscillator calibration that saves post-fabrication test time.

Acknowledgment

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TABLE I: Performance Comparison

	[2]	[5]	[6]	[1]	This Work
Technology	$0.13\mu m$ CMOS	$0.13\mu m$ CMOS	$65nm$ CMOS	$65nm$ CMOS	$40nm$ CMOS
Area (mm^2)	0.073	0.04	0.02	0.011	0.017
Frequency	3.2MHz	14MHz	6.0MHz	12.8MHz	10MHz
Power (μW)	38.4	43.2	100	98.4	20
RMS Jitter	455ps	N/A	88ps	90ps	8.7ps
Variation with VDD	0.8% (1.4-1.6V)	0.32% (1.7-1.9V)	0.52% (1.15-1.35V)	0.14% (1.1-1.5V)	1.1% (3-4.1V)
Calibration	manual	N/A	N/A	N/A	built-in