A 12.5-Gbps, 7-bit Transmit DAC with 4-Tap LUT-based Equalization in 0.13µm CMOS

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***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13µm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.**

I. INTRODUCTION

Random and systematic parameter fluctuations can degrade circuit performance and signal integrity in high-speed transmitters. For example, when multiphase clocks are used for data serialization, uneven clock phase spacing due to random and systematic variations can lead to inter-symbol timing mismatch. Also, DAC current mismatch introduces nonlinear characteristics to the transmitter output that cannot be easily addressed with conventional linear equalization techniques. As transmitter jitter is amplified by channel bandwidth limitations, especially at high data rates [1,2], inter-symbol timing mismatch can further degrade performance. Thus, for high data rate transceivers, compensation of mismatch effects in the transmitter is desirable. Consequently, digitally-assisted analog circuits are commonly used to compensate for within-die imperfections [3].

This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8].

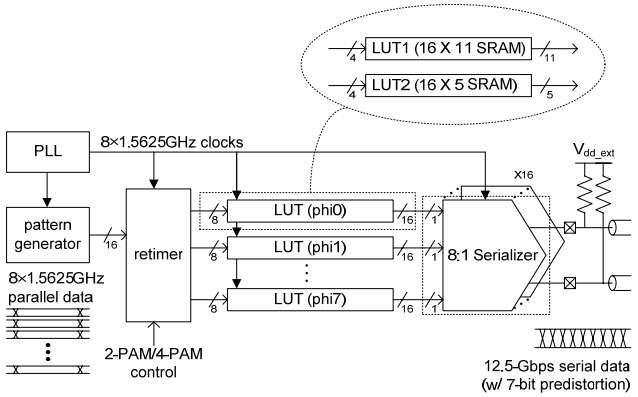

Fig. 1. Overall transmitter block diagram

The remainder of the paper is organized as follows. The next section describes the proposed transmitter architecture and circuits. Section III then provides an analysis of how within-die mismatch affects transmitter performance. Lastly, a description of transmit-side equalization techniques to compensate for various mismatch effects and their measured results are discussed in Sections IV and V, respectively.

II. CIRCUIT DESIGN

Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

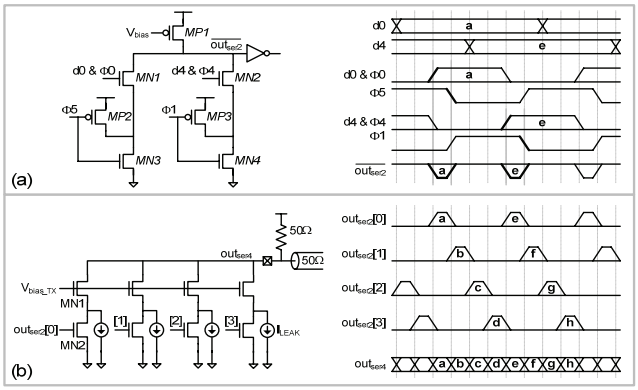

Fig. 2. Two-stage 8:1 serializer schematics and timing diagrams: (a) 2:1 multiplexer and (b) 4:1 multiplexer + current DAC.

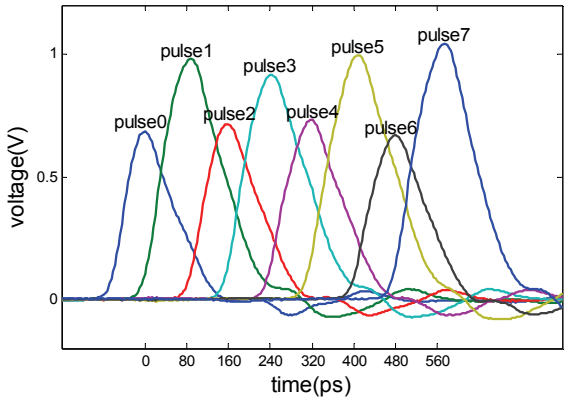

Fig. 3. Transmitter pulse responses through 8 interleaved paths.

higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers.

Fig. 2 illustrates the 8:1 serializer circuitry. To reduce capacitive loading on the output node, serialization occurs in two stages—four parallel 2:1 multiplexers followed by a 4:1 multiplexer combined with the output DAC. Fig. 2(a) shows the circuit schematic and timing diagrams of the 2:1 multiplexing stage. A pseudo-nMOS structure enables high-speed transitions, where pMOS transistors MP2 and MP3 speed up rising transitions and reduce static current in MP1. To eliminate one level of transistor stacking in the final 4:1 multiplexer, otherwise required for delineating each symbol, the 2:1 multiplexer generates pulsed data patterns. Fig. 2(b) shows the circuit schematic and timing diagrams of the subsequent 4:1 multiplexing stage. Leaker devices enable fast switching in each pull-down stack. The 16 parallel sets of 4:1 multiplexer blocks introduce large capacitive loading and, hence, come at the end to leverage the low-impedance output node. A drawback of this highly-parallel structure is its susceptibility to various forms of mismatch and uneven phase spacing between the 8 clocks. On the other hand, the resulting imperfections can be viewed as circuit-induced ISI that the LUT-based equalizer can compensate.

III. WITHIN-DIE MISMATCH EFFECTS

Phase spacing in multiphase clocks are susceptible to random and systematic parameter fluctuations along the clock paths, e.g., inter-stage mismatch in the multi-stage ring oscillator, unbalanced clock distribution network, etc. Unevenly-spaced multiphase clocks can degrade performance in time-division multiplexed (serializing) transmitters due to inter-symbol period mismatch. In the proposed structure, where the 8:1 serializer and transmit DAC are merged together, the effects of uneven phase spacing becomes more serious—both symbol time and voltage swing can vary. Fig. 3 shows the pulse responses of each interleaved transmit path combined to operate at 12.5-Gbps. As shown in the figure, clock phase mismatch leads to irregular widths, heights, and peak positions for the 8 pulses, severely degrading the signal integrity of the transmitter output.

In addition to the phase mismatch across the multiphase clocks, phase mismatch can also be present in the different paths corresponding to the same clock phase. This is mainly due to unbalanced clock loads and wire length mismatch. For example, DAC branches that have smaller load and/or are closer to the clock buffer turn on/off earlier than branches with larger load and/or are farther away from the clock buffer. Such imbalances translate to deviations in the pulse peaks away from ideal positions. As these pulse responses with different peak positions add up at the transmitter output based on different DAC codes, the output pulse peak position also deviates. Fig. 4 presents an overlay of the differential transmitter output of *pulse1* for DAC codes 0 to 127. The X's correspond to the measured peak positions for each code, which exhibits a slight tilt between positive and negative outputs. The vertical line corresponds to the nominal peak position of *pulse1*. Fig. 4(b) presents the INL (error) of the differential DAC output pulses with respect to the peak of each pulse and to a fixed sampling point. The S shape of the INL error curve can be attributed to saturation effects resulting from on-chip bandwidth limitations. Note that these INL results corresponding to high-speed pulses include the effects of mismatch in clock paths and DAC currents. Since we assume symbols are aligned to nominal sampling points, we later calibrate the INL error via LUT code remapping based on the DAC output at the fixed sample point rather than at the peaks of each pulse.

It is difficult to isolate the effects of DAC current mismatch while operating at high frequencies, because clock phase mismatch also affects pulse heights. Hence, we also measured the DAC at a lower frequency (~5 Gbps). Fig. 5 presents the low-frequency DAC INL (error) plot of *pulse1*. Note that the INL error due DAC current mismatch alone is much smaller, within 1 LSB, by avoiding bandwidth limitations from the channel and transmitter circuitry.

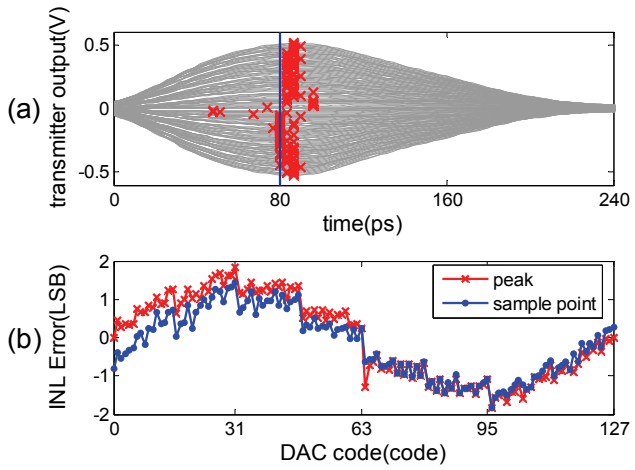

Fig. 4. Effects of within-die mismatch and DAC nonlinearity on pulse1 at 12.5-Gbps: (a) deviations in pulse peak position and (b) 7-bit DAC INL error.

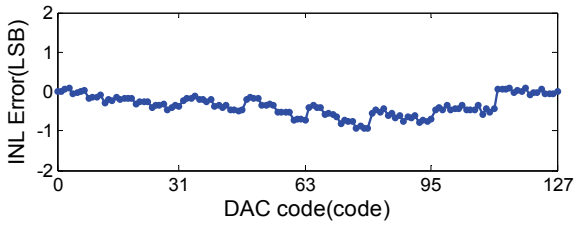

Fig. 5. Effects of DAC current mismatch and nonlinearity on pulse1 at low frequency (~5 Gbps).

IV. EQUALIZATION

While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects.

As shown in Fig. 3, both random and systematic variations can lead to mismatch in the 8 pulse responses corresponding to different serializer paths that present different characteristics and require separate equalization settings for each path. Using 8x8 Multi-Input-Multi-Output (MIMO) mapping [6], each individual pulse response can be treated separately to facilitate finding the appropriate equalization settings. Eq. 1 shows an example of a process to find tap coefficients for a particular pulse (*pulse3*). Note that scaled versions of pulse1, pulse2, and pulse4 are used to cancel out the two post-cursor and one pre-cursor components of *pulse3*, respectively. This conventional equalization technique uses 1x sampling of each cursor and, thus, referred to as 1xEQ.

When the cursors are sampled with evenly spaced time periods, forcing a pre-cursor and two post-cursors to zero can compensate for the effect of uneven phase spacing. However, to compensate for phase mismatch effects even further, Eq. 2

$$\begin{bmatrix} pulse1\ (post2\text{-}cursor) & pulse2\ (post1\text{-}cursor) & pulse3\ (main\text{-}cursor) & pulse4\ (pre\text{-}cursor) \\ \multicolumn{4}{c}{(1x\ sampled\ pulse\ responses)} \end{bmatrix} \begin{bmatrix} w_{post2} \\ w_{post1} \\ w_{main} \\ w_{pre} \end{bmatrix} = \begin{bmatrix} \vdots \\ 0 \\ 0 \\ 1 \\ 0 \\ 0 \\ \vdots \end{bmatrix}. \quad (1)$$

uses mid points between cursors for equalization and requires 2x sampling (2xEQ). In other words, 2xEQ forces inter-symbol data transitions to specific levels.

$$\begin{bmatrix} pulse1\ (post2\text{-}cursor) & pulse2\ (post1\text{-}cursor) & pulse3\ (main\text{-}cursor) & pulse4\ (pre\text{-}cursor) \\ \multicolumn{4}{c}{(2x\ sampled\ pulse\ responses)} \end{bmatrix} \begin{bmatrix} w_{post2} \\ w_{post1} \\ w_{main} \\ w_{pre} \end{bmatrix} = \begin{bmatrix} \vdots \\ 0 \\ 0.5 \\ 1 \\ 0.5 \\ 0 \\ \vdots \end{bmatrix}. \quad (2)$$

To compensate for other within-die mismatch effects, such as DAC nonlinearity and deviations in pulse peak positions, the LUT codes are remapped for each of the 8 individual serializer paths based on DAC INL plots shown in Fig. 4(b).

V. MEASURED RESULTS

A test-chip prototype of the transmitter with LUT-based equalization, fabricated in 0.13µm CMOS, utilizes external termination resistors and voltage to facilitate testing across a wide range of current settings for the DAC at the expense of larger ringing due to parasitic bond wire inductance. In order to reduce ripples caused by bond wire inductance, two 5 ohm resistors were added in series after the differential bond wires and before connecting to the termination resistors.

Fig. 6 shows the eye diagrams of the transmitter output after propagating through a pair of 3-inch coaxial cables and into a high-speed sampling scope while operating at 12.5-Gbps. As shown in Fig. 6(a), 4 out of the 8 eyes are completely closed with any compensation. By treating the internal circuit mismatch as ISI, Figs. 6(b), (c), and (d) show LUT-based equalization can salvage this otherwise unusable transmitter and compensate various within-die mismatch effects. 2xEQ with LUT code remapping provides the best jitter performance as well as the most evenly distributed phase spacing by forcing the data transition position to the mid-point between cursors.

To verify the benefits of forcing data transitions to the mid-point between symbols in 2xEQ, mean and rms jitter of zero crossings while transmitting random data are measured. Fig. 7 shows one of the histograms used for the measurement.

Fig. 8(a) plots the INL (error) of mean data transition positions across 8 symbols when 1xEQ and 2xEQ are applied. Note that results without equalization are not included in the plot, because half of the eyes are completely closed making it impossible to measure zero crossing points. While both 1xEQ and 2xEQ can compensate for phase mismatch effects, 2xEQ

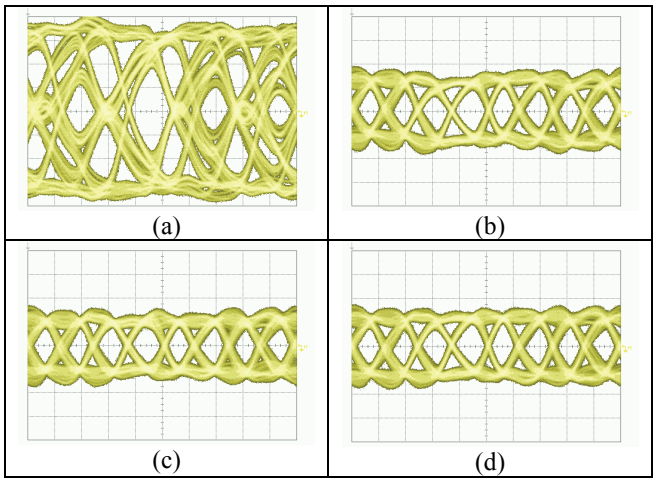

Fig. 6. Eye diagrams of transmitter at 12.5-Gbps: (a) without equalization, (b) with 2xEQ before LUT code remapping, (c) with 1xEQ, and (d) with 2xEQ after LUT code remapping.

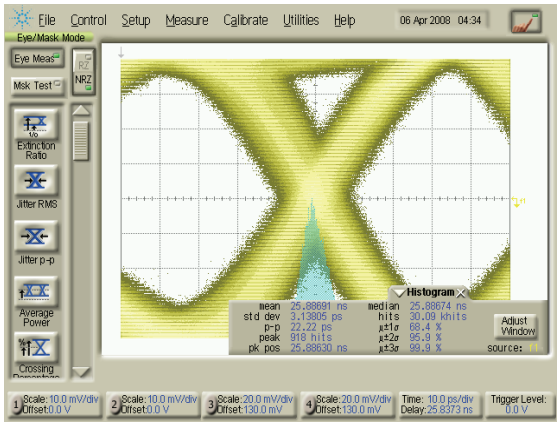

Fig. 7. Histogram of zero crossings for mean and rms jitter measurement.

enables lower average error across the 8 crossings. The standard deviations of INL error for 1xEQ and 2xEQ are 3.43ps and 2.89ps, respectively. The results for 2xEQ before LUT code remapping are also included in Fig. 8 to show that DAC nonlinearity can degrade performance due to inaccurate code settings. The standard deviation of INL error for 2xEQ before LUT code remapping is 2.93ps.

Fig. 8(b) plots the rms jitter at the data crossing across 8 symbols when 1xEQ and 2xEQ are applied. For all the 8 zero crossing points 2xEQ provides better jitter performance compared to 1xEQ. The average RMS jitter for 1xEQ, 2xEQ, and 2xEQ before LUT code remapping are 5.51ps, 4.77ps, and 4.90ps with standard deviation of 1.36ps, 1.19ps, and 0.80ps, respectively. Figs. 8(a) and 8(b) show that 2xEQ with LUT code remapping provides the best equalization setting.

Fig. 9 presents the die photo of the test chip. The overall chip area, including I/O pads, 16 interleaved 16-word SRAMs, and PLL, is 3.08×1.47 mm^2, with 1.03 mm^2 of active area. While operating at 12.5-Gbps off of a 1.2-V supply, the chip consumes 425mW where 36% of this power is consumed in test-related blocks (e.g., pattern generator and retimer).

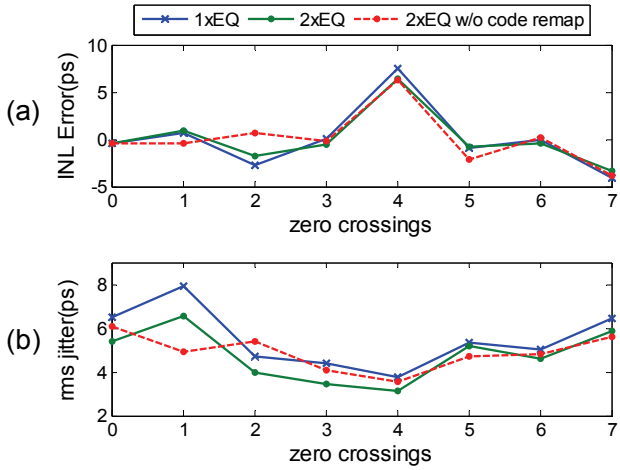

Fig. 8. Data transition point measurements: (a) mean INL error, (b) rms jitter.

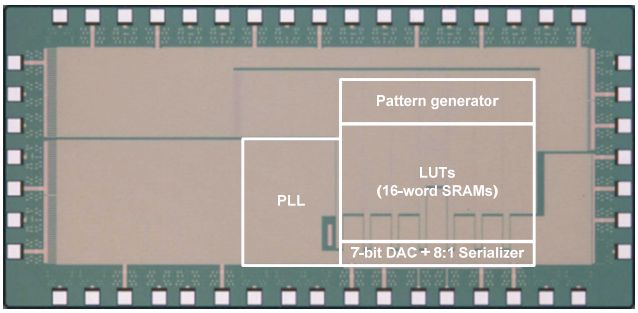

Fig. 9. Die photo and overlay of basic blocks.

ACKNOWLEDGMENTS

This work was supported in part by Samsung and the NSF CCF0325228. The authors also thank UMC for test-chip prototype fabrication.

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