Design of Low-Power Short-Distance Opto-Electronic Transceiver Front-Ends with Scalable Supply Voltages and Frequencies

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ABSTRACT

The need for low-power I/Os is widely recognized, as I/Os take up a significant portion of total chip power. In recent years, researchers have pointed to the potential system-level power savings that can be realized if dynamic voltage scalable I/Os are available. However, substantial challenges remain in building such links. This paper presents the design and implementation details of opto-electronic transceiver front-end blocks where supply voltage can scale from 1.2V to 0.6V with almost linearly scalable bandwidth from 8Gb/s to 4Gb/s, and power consumption from 36mW to 5mW in a 130nm CMOS process. To the best of our knowledge, this is the first circuit demonstration of voltage-scalable optical links. It demonstrates the feasibility of dynamic voltage scalable optical I/Os.

Categories and Subject Descriptors

B.4.3 [**Input/Output and Data Communications**]: Interconnections (subsystems)

General Terms

Design

Keywords

dynamic voltage and frequency scaling, interconnection networks, optical transceiver, voltage-controlled inductive load

1. INTRODUCTION

While optical interconnects are predominantly used for long distance telecommunications, increases in bandwidth demands have motivated the use of optical links in box-to-box interconnects and even in the board-to-board domain as well. In order to replace copper in short distance interconnects, optical links must not only support high data rates but also be low power and low cost. Unfortunately, power consumption of a typical optical link can be quite high [1].

In efforts to optimize power utilization, computer architects have recently proposed building power-aware networks that scale the link voltage at runtime [4, 10, 15, 18] in response to actual traffic in order to scale down power consumption. The basic premise is to use a high supply voltage, needed to deliver high bit rates and bandwidth, when data traffic is high, and use a low supply voltage when traffic is light. These system level studies suggest the potential for large power savings via dynamic voltage and frequency scaling. However, they gloss over the link circuit design issues required to make such power-aware networks possible. Conventional link designs typically assume fixed-voltage operation and do not support runtime scaling across a wide range of supply voltages [3, 6, 13, 16]. Some broadband links [1] support a wide frequency range, but since the power consumption of analog links is dominated by the supply voltage post-fabrication, frequency scaling alone would not lead to any power savings, but will instead hurt performance. To demonstrate the feasibility of power-aware networks using optical links, this paper presents a prototype test chip that implements optical transceiver front-end building blocks—a laser driver and transimpedance amplifier (TIA)—in a 130nm CMOS process. These circuits can operate off of a supply voltage that scales from 1.2 to 0.6V and correspondingly scale bandwidth from 8Gb/s to 4Gb/s, leading to power consumption that scales from 36mW to 5mW.

The rest of the paper is organized as follows. Section 2 provides the details of the proposed circuit implementation for the low-power transmitter front-end. Section 3 then dives into the design details of a low-power receiver front-end and presents techniques to boost gain in an environment where voltages scale down. Section 4 presents experimental results verifying voltage, frequency, and power scalability for optical links. Lastly, Section 5 concludes the paper.

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2. TRANSMITTER FRONT-END

For short-distance optical interconnects, speed, power, cost, and area are all important parameters to consider. Hence, we utilize a VCSEL as the direct-modulated light source in the transmitter [2]. This section details the design of the driver circuitry for the VCSEL. As shown in Fig. 1, the final stage of a VCSEL driver is simply a switched open-drain current source, so our design largely focuses on the pre-amplifiers that drive the current source to the VCSEL. In conventional common-source differential amplifiers with resistor loads, gain and bandwidth do not scale well with supply voltage. To overcome this limitation, we propose circuit techniques that can scale amplifier gain and bandwidth with respect to the supply voltage for use in a system that seeks to scale frequency and voltage for power savings.

2.1 Bandwidth and gain boosting

For the conventional common-source differential amplifier, gain is proportional to $g_m \cdot R$ while the bandwidth is inversely proportional to $C_L \cdot R$. Here $g_m \propto I_b^{1/2}$ is the transconductance of the NMOS, I_b is the bias current of the differential amplifier, R is the load resistance, and C_L is the output load capacitance. R must be large to obtain high gain and suppress the noise introduced by R.

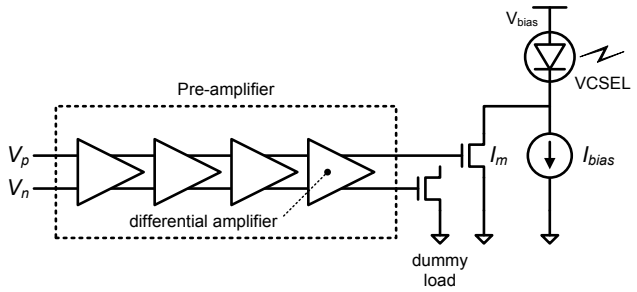


Figure 1: Laser driver block diagram.

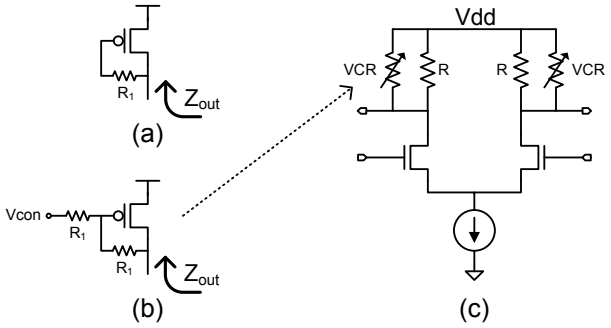


Figure 2: (a) PMOS device configured as active inductor, (b) Inductive voltage-controlled resistor (VCR), and (c) Differential amplifier with voltage-controlled inductive loads.

However, $0.5 \cdot I_b \cdot R$ is also constrained by the low supply voltage in aggressively-scaled process technologies.

A PMOS current source is often added in parallel to R loads to provide a part of the bias current [14]. If the PMOS current source delivers one fourth of the bias current, R could be increased by a factor of two, doubling gain while maintaining the same voltage drop compared to the case without the additional PMOS current source. However, bandwidth is still limited by the larger R. It is well known that inductive peaking can substantially increase the bandwidth of gain stages. To keep chip size small, inductive peaking could be implemented by means of active devices [14]. Fig. 2(a) illustrates one approach to implement an active inductor. To simplify the illustration, gate-drain overlap capacitance, source-bulk capacitance and channel-length modulation are neglected.

$$Z_{out} = r_o \| \frac{(1 + s \cdot R_1 \cdot C_{gs})}{g_m + s \cdot C_{gs}} \quad (1)$$

The load exhibits an impedance, Z_{out} of $\frac{1}{gm} \| r_o$ at low frequencies and $R_1 \| r_o$ at high frequencies. Thus, if $R_1 \gg \frac{1}{gm}$, then $|Z_{out}|$ increases with frequencies, exhibiting inductive behavior.

Since this type of active inductive impedance severely limits voltage headroom, a second R_1 is added to alleviate this constraint and is shown in Fig 2(b). The DC condition of V_{gs} changes from $V_d - Vdd$ to $0.5 \cdot (V_{con} + V_d) - Vdd$. The dependence of V_{gs} on V_d is reduced by one half, greatly mitigating the headroom constraints. The resulting output impedance is then:

$$Z_{out} = r_o \| \frac{R_1 \cdot (2 + s \cdot R_1 \cdot C_{gs})}{1 + R_1 \cdot g_m + s \cdot R_1 \cdot C_{gs}} \quad (2)$$

Notice that $|Z_{out}(s = 0)| = r_o \| \frac{2R_1}{1 + R_1 \cdot gm}$ and $|Z_{out}(s = \infty)| = r_o \| R_1$. If $R_1 \gg \frac{1}{g_m}$, Z_{out} again increases with frequency. So

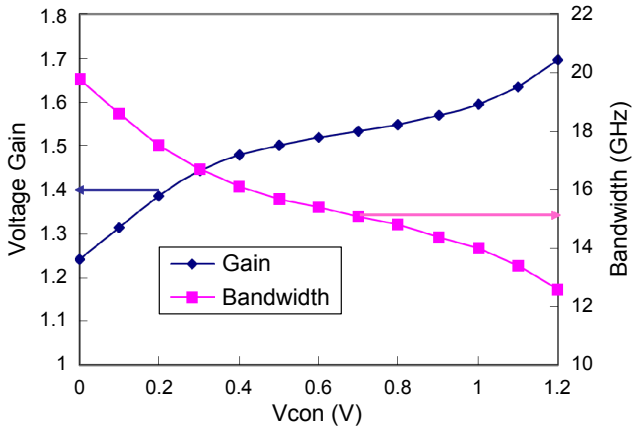


Figure 3: Gain and bandwidth vs. V_{con} for a differential amplifier with voltage-controlled inductive loads, Vdd=1.2V.

properly biasing V_{con} to some voltage lower than V_d, the PMOS remains in saturation, the load circuit shown in Fig. 2(b) acts as a current source with inductive impedance.

This voltage-controlled inductive impedance is added in parallel to each load resistor of the differential amplifier as shown in Fig 2(c). The total load resistance and gain is smaller for lower V_{con} while bandwidth is higher, as shown in Fig 3. To make the control circuit simple, V_{con} can be biased at a fixed voltage, 0V. Even though active inductance can be relatively noisy, signal swings are sufficiently large such that this noise should have small impact on performance.

2.2 Post-layout simulation results

While a fully-integrated design may have larger-swing input signals that feed the laser driver and require fewer buffer stages, in our transceiver front-end, we conservatively assume 200mV low-swing high-speed signals driven by external test equipment to the laser driver. The output load of the laser driver includes the parasitic capacitance of the output pad (100fF) and the VCSEL (200fF) while the parasitic inductance of the bond wires is approximately 1.5nH.

The laser driver was designed in a 130nm CMOS technology. Fig 4 plots the achievable 3dB bandwidth of our laser driver under varying supply voltages from post-layout HSPICE simulations. The plot also includes the voltage-dependent frequency of an inverter-based ring oscillator to illustrate the voltage vs. frequency scaling trend of digital circuitry. Given similar trends, the transmitter can operate in a system where supply voltage is scaled with respect to frequency required by up-stream digital circuits. 5-2.5mA modulation currents are available for supply voltages ranging from 1.2-0.6V, which guarantees enough modulation current to the VCSEL.

Table 1 summarizes the comparison between our proposed laser driver and previous laser driver designs in terms of bit rate, power, and supply voltage range.

3. RECEIVER FRONT-END

On the receiver end, the TIA converts the photodiode current into a voltage that subsequently feeds into a clock and data recovery (CDR) block. Since the CDR consists mostly of digital circuitry, it can operate in a scaled voltage and frequency environment [11, 17]. Hence, we design the TIA to also operate across a wide range of voltages and frequencies in order to reduce power. Moreover, a large transimpedance gain is targeted across the supply voltage range to maintain sufficiently large voltage swings out of the TIA.

Table 1: Comparison of low power laser drivers.

$Bitrate(Gb/s)$	Technology	P(mW)	Supply voltage(V)	Ref
3.5	$0.2\mu m$ CMOS	170	2	[9]
20	$0.13\mu m$ CMOS	70-120	2-2.5	[16]
12.5	$0.09\mu m$ CMOS	27	1	[7]
8-4	$0.13\mu m$ CMOS	27-9	1.2-0.6	This work

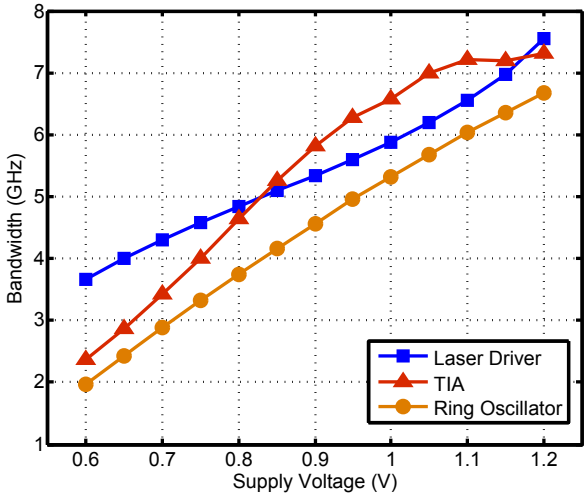


Figure 4: Bandwidth vs. supply voltage of proposed laser driver and TIA compared to the frequency vs. voltage of a 5-stage inverter-based ring oscillator.

There are several challenges to designing a TIA that supports a wide range of frequencies and supply voltages. Since we assume modulation current (I_m) scales with frequency in the transmitter, at low voltages, photon current into the TIA reduces correspondingly. So, transimpedance gain has to be high enough to ensure large output voltage swing. This makes circuit design especially tricky as a reduction in supply voltage also lowers the transimpedance gain, R_f. The TIA design utilizes design techniques that keep transimpedance gain from decreasing at low supply voltages.

3.1 TIA circuit

There are numerous TIA designs for long distance telecommunication links [14]. However, they are mostly fabricated in GaAs, InP, or SiGe technologies, which lead to high power consumption and difficulty in integrating with CMOS designs. Several CMOS TIA designs [5, 6, 8, 12, 13] have been proposed for low power, short-distance optical links in the past few years, but they do not support operation across a wide range of supply voltages—circuit bandwidths will severely degrade at lower voltages, making them inoperable even at lower bit rates. Furthermore, many high-bandwidth TIAs use on-chip spiral inductors to boost link bandwidth. Such inductors cannot be readily scaled with respect to supply voltage and frequency, and substantially increase circuit footprint.

We explored several TIA structures, before choosing the single-ended common-gate feed-forward TIA design [13], as shown in Fig. 5(a), as a starting point since it offers high bandwidth and low power operation while requiring low voltage headroom. However, there are several limitation that must be addressed. First, this circuit does not support wide supply voltage range operation. The transimpedance gain was only $52db\Omega$ *or* 400Ω, which requires multiple post amplifiers before feeding into the CDR and, thus, higher power consumption. More importantly, the transimpedance gain reduces as supply voltage scales down. Lastly, passive inductors were used in this design to boost the bandwidth. Just as we explored the use of inductive loads to boost the bandwidth of pre-amplifier stages in the laser driver, we investigate how they can be applied to boost gain in the TIA.

3.2 Gain boosting

An important design target for the TIA is to ensure that transimpedance gain does not decrease when the supply voltage is scaled down in order to guarantee minimum voltage margins for the downstream CDR circuitry. Transimpedance gain R_{TIA} can be calculated from small signal analysis as follows:

$$R\_\{TIA\}(s{=}0) = \frac{R_1}{1+\frac{g_{m2}}{g_{m1}(1+g_{m2}R_2g_{m3}R_3)}} \quad (3)$$

At high supply voltages, with $1 + g_{m2}R_2g_{m3}R_3 \gg 1$, $R_{TIA} \approx R_1$. When supply voltage scales down, $\frac{g_{m2}}{g_{m1}(1+g_{m2}R_2g_{m3}R_3)}$ can be comparable to 1, thus reducing R_{TIA} to half R_1 or even lower, which is not desirable.

From Equation 3, there are two ways to boost transimpedance gain at low supply voltages. One straightforward approach is to increase R_1. Simply increasing R_1, however, will reduce the bandwidth at high supply voltages since bandwidth is inversely proportional to R_1. An alternative approach is to keep g_{m1}, g_{m2}, g_{m3} high even at low supply voltages, but this comes with its own share of challenges, as the load resistor is large and requires considerable voltage drop across it. We choose the latter approach in our design.

Our design, shown in Fig. 5(b), inserts voltage-controlled inductive loads R_v (see Fig. 2) in parallel to the load resistors to raise the total resistance at low supply voltages while keeping all transistors in saturation.

$$R\_\{v\}(s{=}0) = r_o \| \frac{2R_1}{1+R_1 \cdot gm} \quad (4)$$

Since gm will decrease when supply voltage scales down, R_v will increase. The load resistance in the input stage $R_1 \parallel R_v$ will also increase a little when supply voltage decreases. In addition, since there is now a PMOS transistor in parallel with the load resistor R_1 to share the current, the voltage drop across R_1 is reduced. $Vdd = R_1 \times I_{R1} + V_{ds1} + V_{ds0}$. As a result, there is more voltage room to keep the transistors in saturation and keep g_{m1}, g_{m2}, g_{m3} large. In this way, it is now possible to have high transimpedance gain even when supply voltage scales down, thereby averting the need for multiple stages of post amplifiers.

3.3 Post-layout simulation results

Fig 6 presents post-layout HSPICE simulations of transimpedance gain for the TIA across a range of supply voltages, including parasitics from post-layout extraction. The output load of the TIA is assumed to be $50fF$, representing the loading imposed by the clock data recovery circuity (CDR). The input load includes the large capacitance associated with the photo-detector (300fF) and the input

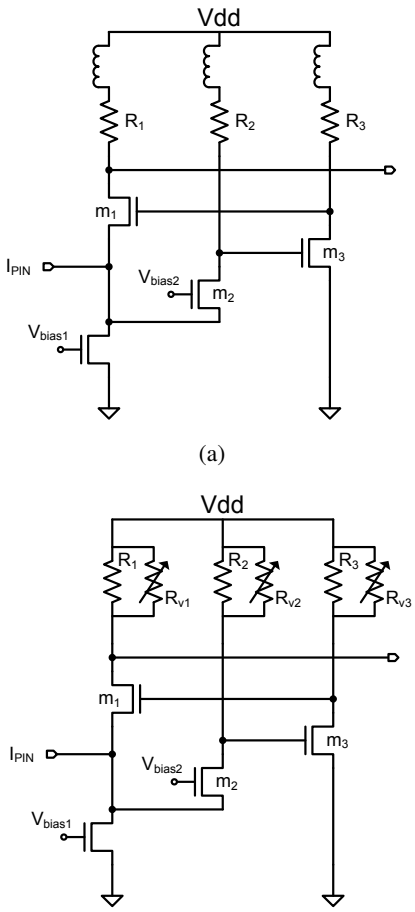


Figure 5: Schematic of (a) common-gate feed-forward TIA with inductive peaking and (b) proposed TIA with voltage-controlled inductive loads.

pad (100fF). We assume parasitic bond wire inductance of $1.5nH$. Fig 4 presents the achievable $3db$ bandwidth across a range of supply voltages. The transimpedance gain of our TIA is more than 800Ω for low supply voltages, which assures high output swing for the CDR. Again, similar frequency vs. voltage trends suggest this circuit can be used in a system that scales supply voltage with respect to frequency for digital circuits.

Fig 7 shows the eye diagram for the TIA operating at different supply voltage and bit rates. The input photon current is 0.2mA at 1.2V and, 0.15mA at 0.7V. There are wide open eyes with more than large voltage swings ($> 100mV$) for both supply voltages. Table 2 compares our TIA with previous TIA designs in terms of bit rate, transimpedance gain, power, and supply voltage range.

4. EXPERIMENTAL RESULTS

The test-chip prototype was fabricated in a 130nm CMOS logic process. Fig 8(a) shows the die photo of the transceiver front-ends with laser driver and TIA blocks highlighted. The total chip area is 1mm X 1.5mm where laser driver is about $40\mu mX150\mu m$ and TIA is about $40\mu mX35\mu m$. The fabricated chip is directly bonded onto the PCB. Testing was performed in an optical lab with off-chip photodiode and VCSEL connected via impedance-controlled channels on the board.

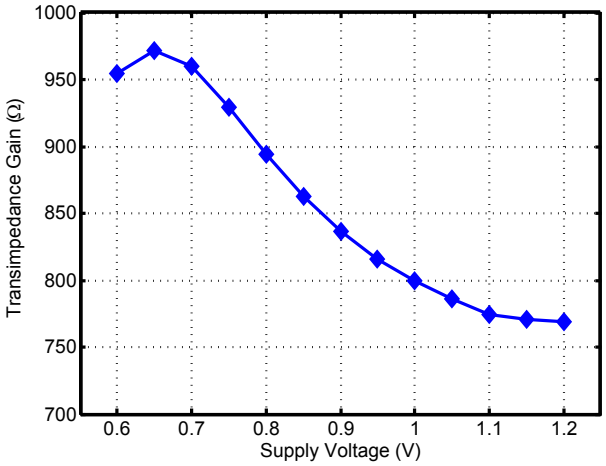
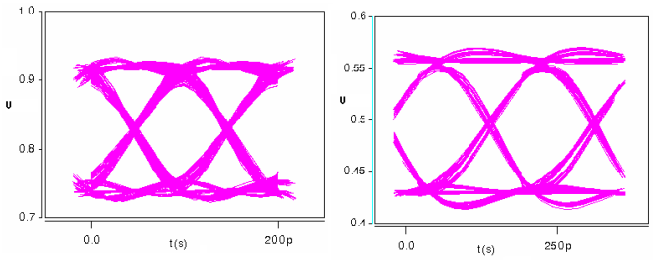


Figure 6: Simulated transimpedance gain versus supply voltage for the proposed TIA with voltage-controlled inductive loads.



(a) Vdd=1.2V, BR=10Gb/s, P=2.2mW

(b) Vdd=0.7V, BR=5Gb/s, P=0.5mW

Figure 7: Simulated eye diagrams of proposed TIA at (a) Vdd=1.2V, 10Gb/s (b) Vdd=0.7V, 5Gb/s.

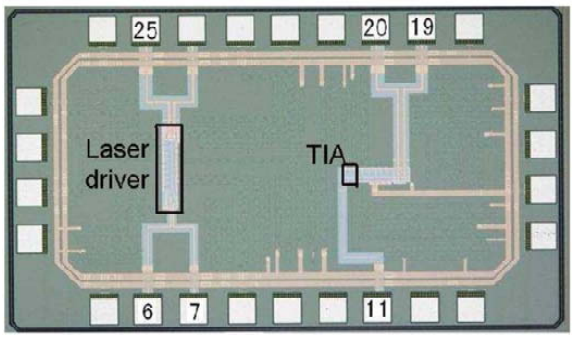
We originally planned to test the transceiver front-ends as a full link system—with the transmitter front-end driving the VCSEL and the photodiode converting light from the VCSEL to input photon current to the received front-end, which transforms the photon current into the amplified voltage signal. A 10Gb/s 850nm VCSEL with a multi-mode fiber pig tail is used as the laser for the transmitter front-end. Unfortunately, we were unable to purchase a packaged 850nm photodiode for the receiver front-end, and instead, had to use a 10Gb/s 1550nm photodiode to test the receiver. While all 1550nm photodiodes work with single-mode fiber and have a low conversion rate at 850nm wavelength, we are unable to test the transceiver front-ends as a single system, since large loss in the optical channel masks achievable operation.

The voltage inputs to the laser driver are differential PRBS (pseudo random bit sequence) signals from an external signal generator. Modulation current of the laser driver is tested by monitoring voltage across a 50Ω termination resistor under different supply voltages and bit rates using an oscilloscope. Since the input port of the oscilloscope is terminated to ground by a 50Ω resistor, a bias tee is inserted between the output of the laser driver and input port of the oscilloscope to block the DC level. The bias tee is built on the PCB with a 0.22μF capacitor and a 470μH inductor. Fig. 9 presents the eye diagram of the modulation current times 50Ω termination at 1.2V, 6Gb/s and 0.6V, 4Gb/s. The modulation current scales from 5mA to about 2.5mA when supply voltage scales from 1.2V to 0.6V.

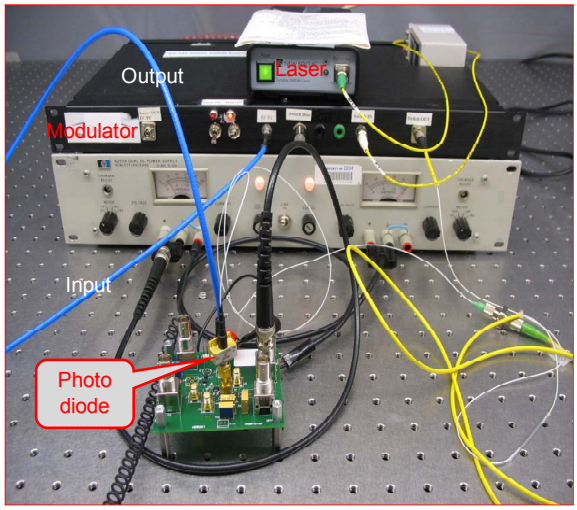
The input to the receiver front-end is the photon current from the photodiode with light input at approximately -10dbm. Photon cur-

Table 2: Comparison of high speed transimpedance amplifiers.

$Bitrate(Gb/s)$	Technology	R(Ω)	P(mW)	Supply voltage(V)	Ref
2.6	0.18μm CMOS	861	47	1.8	[3]
10	0.1μm CMOS	200	15	1.0	[6]
19	80nm CMOS	178	6.5	1.0	[12]
20	80nm CMOS	400	2.2	1.0	[13]
8-4	0.13μm CMOS	900-700	2.2-0.5	1.2-0.6	This work



(a) Die photo



(b) Test setup

Figure 8: Test-chip prototype die photo and TIA test setup.

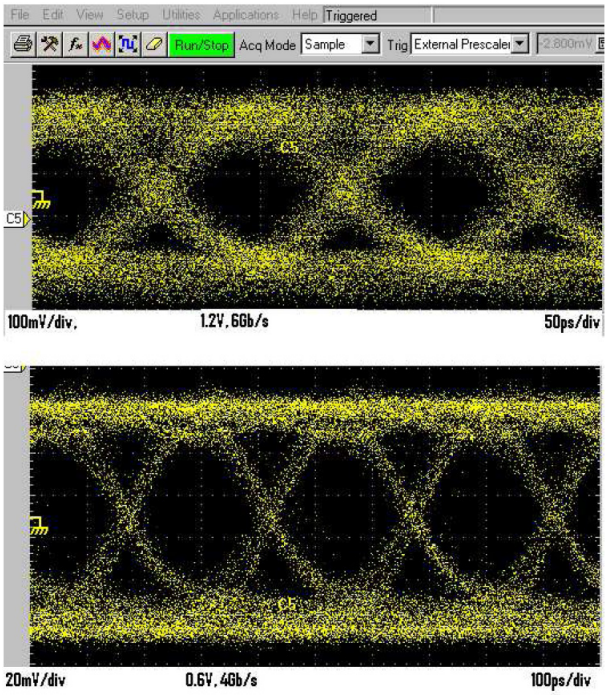


Figure 9: Eye diagrams of modulation current with 50Ω termination for Vdd=1.2V and Vdd=0.6V, respectively.

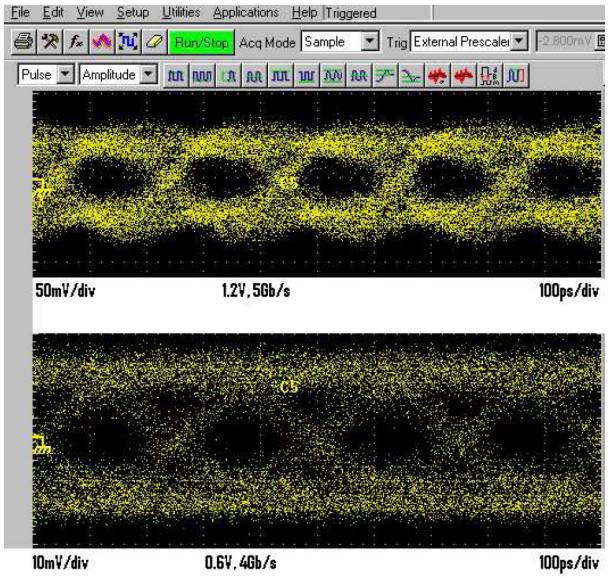


Figure 10: Measured eye diagram of receiver front-end at 1.2V and 0.6V.

rent is converted into a voltage signal by the TIA. Then several post amplifiers and output buffer are used to drive the TIA output of the chip for testing. The test setup of the receiver front-end is shown in Fig. 8(b). Since the photodiode is terminated to ground by a 50Ω resistor to achieve high bit rates, an on-board DC blocking capacitor (0.22μF) is inserted between the photodiode and the TIA. Fig. 10 shows the eye-diagram of the output at 1.2V, 5Gb/s and 0.6V, 4Gb/s.

Power consumption of the entire test board is measured under different supply voltages. As shown in Fig. 11, power consumption scales from 36mW to 5mW when supply voltage scales from 1.2V to 0.6V. The testing results show power consumption is roughly proportional to Vdd^2, confirming that substantial power savings could be achieved by voltage scaling.

According to the post layout simulation results, the 3dB bandwidth at 1.2V for both layer driver and receiver front-ends are more than two times larger than the bandwidth at 0.6V as shown in Fig. 4. However, the limitations of both PCB technology and the test equipments prevent clean measurements beyond 5Gb/s. Besides, larger

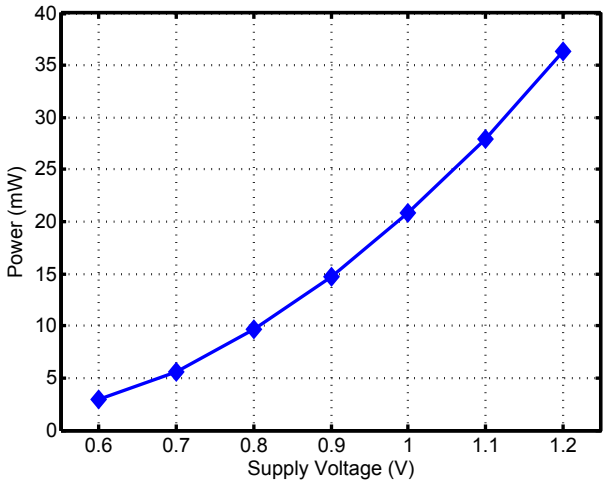


Figure 11: Total power consumption vs. supply voltage.

than expected bonding wire inductance from chip to board ($>$ 2nH) also constrains high-frequency operation. So test measurements show that our transceiver front-ends works well at 4Gb/s at 0.6V, but the bit rates can not goes up at 1.2V as we expected. We believe that our transceiver front-ends chip can work at bit rates higher than 8Gb/s at 1.2V with bare-die testing.

5. CONCLUSIONS

In pursuit of power-aware networked systems, this paper presents designs for low-power transceiver front-end circuits that enables opto-electronic links to track traffic utilization and benefit from voltage and bit rate scaling to minimize power consumption. To the best of our knowledge, this is the first design of transceiver front-ends which can support wide supply voltage ranges. In 130nm CMOS technology, our laser driver and TIA maintains high gain and high bandwidth across the entire supply voltage range from 1.2V to 0.6V. Bandwidth scales linearly with supply voltage while power consumption scales with Vdd^2 from 36mW to 5mW. In addition, there are no on-chip spiral inductors in our high bandwidth transceiver front-ends. More importantly, with voltage-controlled inductive loads, high gain is maintained for the TIA across the entire voltage range, which is crucial for the voltage scaling of the optical link. Clearly, more work needs to be done before a complete dynamic voltage scalable link can be realized. However, we believe our work marks an important step towards demonstrating the feasibility of dynamically-scalable low-power optical links.

Acknowledgments

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6. REFERENCES

[1] AFL3430 RF Fiber Optic Link. `http://www.endruntechnologies.com/fiber-optic-link.htm`.

[2] VCSEL XM85 R5P0U. `http://www.roithner-laser.com/All_Datasheets/VCSELs/XM85-R5P0U.pdf`.

[3] F. Beaudoin and M. N. El-Gamal. A 5-gbit/s cmos optical receiver front-end. In *IEEE Int. Midwest symp. Circuit and Systems*, volume 3, 2002.

[4] X. Chen, L.-S. Peh, and G.-Y. Wei. Explore the design space of power aware opto-electronic networked system. In *Proc. Int. Symp. High Performance Computer Architecture*, Feb. 2005.

[5] C.Hermans and M.Steyaert. A high speed 850-nm optical receiver front-end in 0.18-um cmos. *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, 41(7):1606–1614, July 2006.

[6] T. K. f. Pailler. Low power and noise tolerant 20gb/s cmos tia for short distance optical interconnect. *Mixed-signal Design*, pages 49–53, Feb 2003.

[7] G.Sialm, C. Kromer, F. Ellinger, and T. Morf. Design of lower power fast vcsel drivers for high-density links in 90-nm soi cmos. *IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES*, 54(1):65–73, JANUARY 2006.

[8] D. Guckenberger, J. D. Schaub, and K. T. Kornegay. A dc-coupled low-power transimpedance amplifier architecture for gb/s communication system applications. *IEEE Radio Frequency Integrated Circuit Symposium*, pages 515–518, June 2004.

[9] K. Iga. Vertical cavity surface emitting laser: introduction and review. *Vertical cavity surface emitting laser devices*, pages 1–27, 2003.

[10] E. J. Kim, K. H. Yum, G. M. Link, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, M. Yousif, and C. R. Das. Energy optimization techniques in cluster interconnects. In *Proc. Int. Symp. Low Power Electronics and Design*, pages 459–464, Aug. 2003.

[11] J. Kim and M. Horowitz. Adaptive supply serial links with sub-1V operation and per-pin clock recovery. In *Proc. Int. Solid-State Circuits Conf.*, pages 216–221, Feb. 2002.

[12] M. Kossel, C. Menolfi, T. Morf, M. Shmatz, and T. Toifl. Wideband cmos transimpedance amplifier. *ELECTRONICS LETTERS*, 39(7):587–588, April 2003.

[13] C. Kromer, G. Sialm, T. Morf, M. Schmatz, F. Ellinger, D. Erni, and H. Jackel. A low power 20-ghz 52-db ω transimpedance amplifier in 80-nm cmos. *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, 39(6):885–893, June 2004.

[14] B. Razavi. Design of integrated circuits for optical communications. pages 103–104.

[15] L. Shang, L.-S. Peh, and N. K. Jha. Dynamic voltage scaling with links for power optimization of interconnection networks. In *Proc. Int. Symp. High Performance Computer Architecture*, pages 79–90, Feb. 2003.

[16] J. Simon, S. R. L. Windower, K. Giboney, B. Law, g. Flower, L.Mirkarimi, A. Grot, C. k. Lin, A. Tandon, G. Rankin, R. Gruhlke, and D.Dolfi. Parallel optical interconnect at 10gb/s per channel. *IEEE Electronic Components and Technology Conf.*, pages 1016–1023, 2004.

[17] G. Wei, J. Kim, D. Liu, S. Sidiropoulos, and M. Horowitz. A variable-frequency parallel I/O interface with adaptive power-supply regulation. *Journal of Solid-State Circuits*, 35(11):1600–1610, Nov. 2000.

[18] F. Worm, P. Ienne, P. Thiran, and G. De Micheli. A robust self-calibrating transmission scheme for on-chip networks. *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, 13(1):126–139, Jan. 2005.