Chapter 3

POWER-EFFICIENT ISSUE QUEUE DESIGN

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Abstract Increasing levels of power dissipation threaten to limit the performance gains of future high-end, out-of-order issue microprocessors. Therefore, it is imperative that designers devise techniques that significantly reduce the power dissipation of the key hardware structures on the chip without unduly compromising performance. Such a key structure in out-of-order designs is the issue queue. Although crucial in achieving high performance, the issue queues are often a major contributor to the overall power consumption of the chip, potentially affecting both thermal issues related to hot spots and energy issues related to battery life. In this chapter, we present two techniques that significantly reduce issue queue power while maintaining high performance operation. First, we evaluate the power savings achieved by implementing a CAM/RAM structure for the issue queue as an alternative to the more power-hungry latch-based issue queue used in many designs. We then present the microarchitecture and circuit design of an adaptive issue queue that leverages transmission gate insertion to provide dynamic low-cost configurability of size and speed. We compare two different dynamic adaptation algorithms that use issue queue utilization and parallelism metrics in order to size the issue queue on-the-fly during execution. Together, these two techniques provide over a 70% average reduction in issue queue power dissipation for a collection of the SPEC CPU2000 integer benchmarks, with only a 3% overall performance degradation.

1. Introduction

Power dissipation has become a major microprocessor design constraint, so much so that it threatens to limit the amount of hardware that can be included

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year	1999	2002	2005	2008	2011	2014
feature size (nm)	180	130	100	70	50	35
logic trans/cm^2	6.2M	18M	39M	84M	180M	390M
clock (MHz)	1250	2100	3500	6000	10000	16900
chip size (mm^2)	340	430	520	620	750	900
power supply (V)	1.8	1.5	1.2	0.9	0.6	0.5
high-perf power (W)	90	130	160	170	175	183

Table 3.1. SIA Roadmap for Power Dissipation in Current and Future Microprocessors

on future microprocessors how fast it can be clocked [11, 12, 14]. Designers of handheld devices are already quite familiar with the difficulties in meeting ever-increasing performance demands while maintaining reasonable battery life and small product form-factors. However, the increasing packaging, cooling, and power distribution costs, as well as reliability issues, associated with increasing power dissipation in high-end systems also threatens their future viability.

Table 3.1 summarizes the SIA Roadmap [18] for power dissipation in current and next generation high-performance microprocessors. According to these projections, power dissipation will increase from 90 watts in 1999 to 170 watts in 2008. Clearly, rapid increases in both the clock frequency and chip functionality (complexity) are outpacing circuit and microarchitectural design attempts to maintain reasonable power dissipation limits.

One of the major contributors to the overall power consumption in a modern out-of-order superscalar processor, like the Alpha 21264 and Mips R10000 [13, 16], is the issue queue. The issue queue holds decoded and renamed instructions until they issue to appropriate functional units. The choice of an issue queue size requires striking a careful balance between the ability to extract instruction-level parallelism (ILP) from common programs and achieving high frequency operation. The size of the issue queue represents the *window* of instructions that may be eligible at any given cycle for issue. An instruction residing in the issue queue becomes eligible for issue (or *woken up*) when both of its source operands have been produced and an appropriate functional unit has become available. The *selection logic* determines which instructions (up to maximum issue width of the processor) should issue out of those woken up on a given cycle. Many superscalar processors such as the Alpha 21264 [13] and MipsR10000 [16] use multiple issue queues tailored to the type of instruction (*e.g.*, integer, floating point, and memory). Because the issue queue can be a major contributor to overall power dissipation (for instance, the integer queue on the Alpha 21264 is the highest power consumer on the chip [15]),